MECL

INTEGRATED CIRCUITS
MC300/MC350 SERIES

MECL

INTEGRATED CIRCUITS

INDEX
MC300 Series

NUMERICAL INDEX
(Functions and Characteristics)

$V_{CC} = 0$, $V_{EE} = -5.2$ V, $T_A = 25^{\circ}C$

Function	Type ①	DC Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg	Case	Page No.
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R-S Flip-Flop	MC302		11	42		2-20
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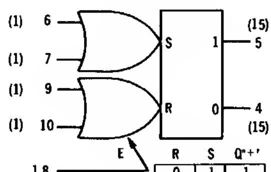
① G suffix denotes Metal Can, F suffix denotes Flat Package. (i.e., MC301G = Metal Can, MC301F = Flat Package.)
② With 93-ohm load (each side)

POSITIVE LOGIC: V_H is a logical "1", V_L is a logical "0"
NEGATIVE LOGIC: V_H is a logical "0", V_L is a logical "1"

The logic diagrams shown describe the circuits of the MC300 line and permit quick selection of those circuits required for the implementation of this particular logic system. Pertinent information such as logic equations, typical time delay, typical power dissipation, and truth tables is provided to show line compatibility. Package pin numbers and fan-in and fan-out for each device are specified on each logic diagram. The numbers at the ends of the terminals are package pin numbers. The numbers in parentheses indicate ac loading factors at each terminal.

MECL circuits require a bias voltage which, for best results, should be obtained from a regulated, temperature-compensated, bias supply. A bias driver, type MC304, is included in the MECL line to provide this function when the bias driver is not contained in the logic element. Specifications for the bias driver are given on page 2—29.

MC302 — R-S FLIP-FLOP

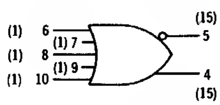


R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

t_{dr} = 10.5 ns
P_D = 42 mW

OC Set-Reset flip-flop with expandable input and buffered outputs.

MC301 — 5-INPUT GATE



$5 = \overline{6 + 7 + 8 + 9 + 10}$
$4 = 6 + 7 + 8 + 9 + 10$

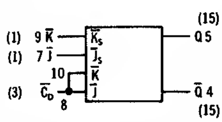
t_{dl} = 7.5 ns
P_D = 37 mW

Provides the positive logic "NOR" function and its complement simultaneously.

MC308 — AC-COUPLED J-K FLIP-FLOP

CLOCKED J-K OPERATION

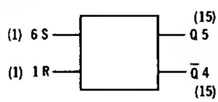
$\overline{J}_S$	$\overline{K}_S$	$\overline{C}_D$	Q^{n+1}
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n



The $\overline{J}_S$ and $\overline{K}_S$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}_S$ and $\overline{K}_S$ inputs would be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} — 0.6 volts)

R-S OPERATION

R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



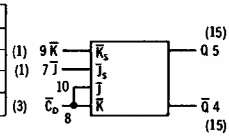
t_{dr} = 7.5 ns
P_D = 87 mW

AC-Coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.

MC314 — AC-COUPLED J-K FLIP-FLOP

CLOCKED J-K OPERATION

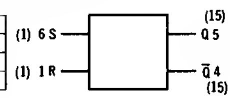
$\overline{J}$	$\overline{K}$	$\overline{C}$	Q^{n+1}
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n



The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} — 0.6 volts)

R-S OPERATION

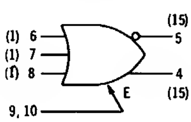
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



t_{dr} = 12 ns
P_D = 118 mW

High-speed ac-coupled J-K flip-flop with dc Set and Reset inputs for counter and shift register applications up to 30 MHz operation.

MC306 — 3-INPUT GATE

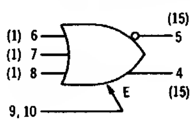


$= \overline{6 + 7 + 8}$
$= 6 + 7 + 8$

t_{dl} = 6.0 ns
P_D = 37 mW

Provides the positive logic "NOR" function and its complement simultaneously.

MC307 — 3-INPUT GATE

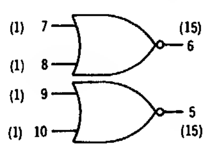


$= \overline{6 + 7 + 8}$
$= 6 + 7 + 8$

t_{dl} = 6.0 ns *No pull-down resistors
P_D = 15 mW

Provides the positive logic "NOR" function and its complement simultaneously. Same as MC306, with pull-down resistors omitted, permitting a reduction of power dissipation (see schematic diagram on page 2-9)

MC309 — DUAL 2-INPUT GATE

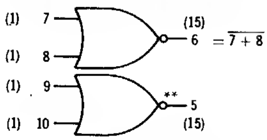


$= \overline{7 + 8}$

t_{dl} = 6.5 ns
P_D = 27 mW/gate

Provides the positive logic "NOR" function.

MC310 — DUAL 2-INPUT GATE

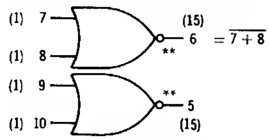


**Optional pull-down resistor. If resistor is desired, connect pin 4 to pin 5.

$t_{d1} = 6.5$ ns $P_D = 27$ mW/gate

Provides the positive logic "NOR" function. Same as MC309 with one output pull-down resistor optional (see schematic diagram on page 2-14).

MC311 — DUAL 2-INPUT GATE

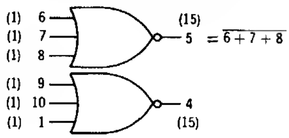


**Optional pull-down resistor If resistor is desired, connect pin 4 to pin 5 or pin 6.

$t_{d1} = 6.5$ ns $P_D = 21$ mW/gate

Provides the positive logic "NOR" function. Same as MC309 with one output pull-down resistor omitted and the second optional (see schematic diagram on page 2-14).

MC312A — DUAL 3-INPUT GATE

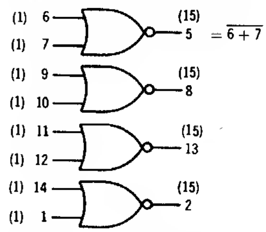


$t_{d1} = 6.5$ ns

$P_D = 35$ mW/gate

Provides the positive logic "NOR" function, and features an internal bias driver. This gate without the bias driver is available as the MC312.

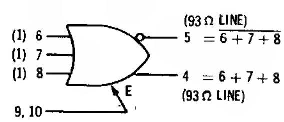
MC313F — QUAD 2-INPUT GATE



$t_{d1} = 6.5$ ns $P_D = 31$ mW/gate

Provides the positive logic "NOR" function, and features an internal bias driver.

MC315 — LINE DRIVER

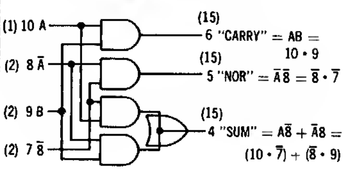


$t_{d1} = 14$ ns

$P_D = 180$ mW (with 93 Ω load)

Drives lines of 93 ohms or greater while providing the positive logic "NOR" function and its complement simultaneously.

MC303 — HALF-ADDER

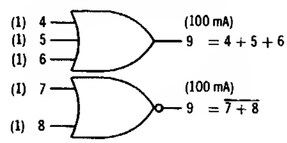


$t_{d1} = 7$ ns

$P_D = 63$ mW

Provides the "SUM", "CARRY", and "NOR" functions simultaneously. If complement inputs are not used, an undefined state can occur.

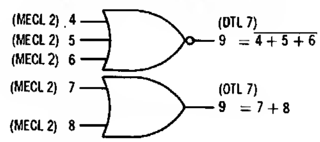
MC316 — LAMP DRIVER



$P_D = 135$ mW

Capable of driving 6-volt lamps. Positive "NOR" function is obtained by applying V_{EE} to pin 4, 5, or 6, with pins 7 and 8 used as inputs. Positive "OR" is obtained by applying V_{EE} to pin 7 or 8, with pins 4, 5, and 6 used as inputs.

MC317 — LEVEL TRANSLATOR

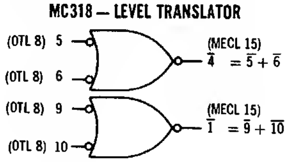


$t_{dr} = 30$ ns

$P_D = 63$ mW

Intended for converting non-saturated MECL signal levels to saturated logic levels. Positive "NOR" function is obtained by applying V_{EE} to pin 7 or 8, with pins 4, 5, and 6 used as inputs. Positive "OR" is obtained by applying V_{EE} to pin 4, 5, or 6, with pins 7 and 8 used as inputs.

MC318 — LEVEL TRANSLATOR

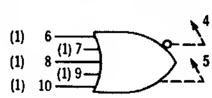


$t_{d1} = 17$ ns

$P_D = 105$ mW

Intended for converting saturated logic levels to non-saturated MECL signal levels. By applying OTL input logic levels as defined by logical "0" at 0.4 V and logical "1" at 5.0 V, corresponding MECL outputs are obtained as defined by logical "0" at −1.55 V and logical "1" at −0.75 V.

MC305 — 5-INPUT EXPANDER



$t_{d1} = 5$ ns

For use with the MC302, MC306, MC307, and MC315. Each expander unit increases the fan-in of the basic gate by five. For highest performance, a maximum of three expander units per gate is recommended.

Note:

Any unused input should be connected to V_{EE}.

CIRCUIT DESCRIPTION

The MECL line of monolithic integrated logic circuits was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic, and permits extremely high-speed operation.

The typical MECL circuit comprises a differential-amplifier input, with emitter-follower output to restore dc levels. High fan-out operation is possible because of the high input impedance of the differential amplifier and the low output impedance of the emitter followers. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the function and its complement.

POWER-SUPPLY CONNECTIONS

Any one of the power supply nodes, V_{BB}, V_{CC}, or V_{EE} may be used as ground; however, the manufacturer has found it most convenient to ground the V_{CC} node. In such a case: $V_{CC} = 0$, $V_{BB} = -1.15$ V, $V_{EE} = -5.2$ V, as shown in the schematic diagram above.

SYSTEM LOGIC SPECIFICATIONS

The output logic swing of 0.8 V then varies from a low state of $V_L = -1.55$ V to a high state of $V_H = -0.75$ V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's". Then

$$\left.\begin{array}{l}\text{"0"} = -1.55\text{ V}\\ \text{"1"} = -0.75\text{ V}\end{array}\right\}\ \text{typical}$$

Dynamic logic refers to a change of logic states. Dynamic "0" is a negative going voltage excursion and a dynamic "1" is a positive going voltage excursion.

CIRCUIT OPERATION

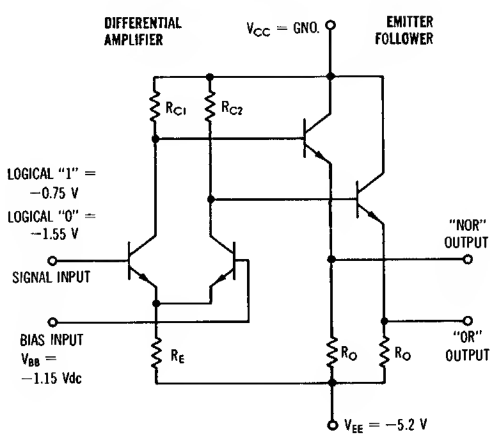
A bias of −1.15 volts is applied to the "bias input" of the differential amplifier and the logic signals are applied to the "signal input". If a logical "0" is applied, the current through R_E is supplied by the fixed-biased transistor. A drop of 800 mV occurs across R_{C2}. The OR output then is −1.55 V, or one V_{BE}-drop below 800 mV. Since no current flows in the "signal input" transistor, the NOR output is a V_{BE}-drop below ground, or −0.75 volts. When a logical "1" level is applied to the "signal input", the current through R_{C2} is switched to the "signal input" transistor and a drop of 800 mV occurs across R_{C1}. The OR output then goes to −0.75 volts and the NOR output goes to −1.55 volts.

Note: Any unused input should be connected to V_{EE}.

BIAS VOLTAGE SOURCE

The bias voltage applied to the bias input is obtained from a regulated, temperature-compensated bias driver, type MC304. The temperature characteristics of the bias driver compensate for any variations in circuit operating point over the temperature range or supply voltage changes, to insure that the threshold point is always in the center of the transition region. The bias driver can be used to drive up to 25 logic elements and should be employed for all elements except those with built-in bias networks.

BASIC MECL GATE CIRCUIT



FOR LOGICAL "1" INPUT, "NOR" OUTPUT = −1.55 V
"OR" OUTPUT = −0.75 V

FOR LOGICAL "0" INPUT, "NOR" OUTPUT = −0.75 V
"OR" OUTPUT = −1.55 V

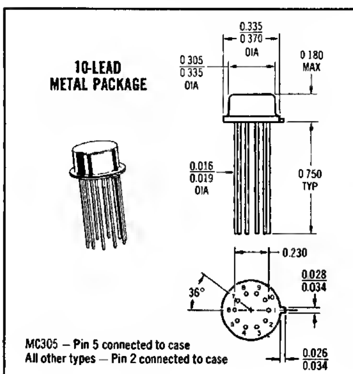
DEFINITIONS

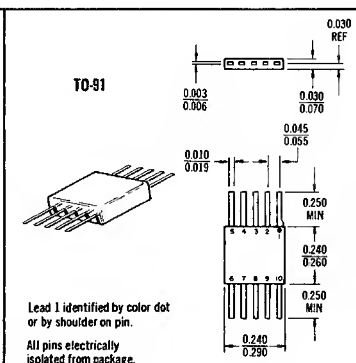
- e_{in} AC signal applied to the input
- e_{out} AC signal at the output
- I_C Amount of current drawn from the positive power supply by the test unit
- I_{CEX} Total collector leakage current exhibited by the gate expander when all inputs are at the negative supply potential
- I_E Amount of current drawn from the test unit by the negative power supply
- I_{in} Current drawn by the input of the test unit when a logical "1" (V_H) is applied to the input
- I_L Current drawn from a node when that node is at ground potential
- t_{d1} Time required for the output pulse to reach the 50% point of its leading edge when referenced to the 50% point of the input pulse leading edge
- t_{d2} Time required for the output pulse to reach the 50% point of its trailing edge when referenced to the 50% point of the input pulse trailing edge
- t_{df} Time required for a flip-flop output to reach the 50% point of its negative going edge when referenced to the 50% point of the input pulse leading edge
- t_{dr} Time required for a flip-flop output to reach the 50% point of its positive going edge when referenced to the 50% point of the input pulse leading edge
- t_f Time required for the output pulse to go more negative from its 90% point to its 10% point
- t_r Time required for the output pulse to go more positive from its 10% point to its 90% point
- V_1 "NOR" output voltage – logical "1" level output voltage when a logical "0" level (V_L) is applied to the input
- V_2 "OR" output voltage – logical "0" level output voltage when a logical "0" level (V_L) is applied to the input
- V_3 Saturation breakpoint voltage which corresponds to the "NOR" output characteristic where the rate of change in the output voltage to the rate of change in input voltage is zero
- V_4 "NOR" output voltage – logical "0" level output voltage when a logical "1" level ($V_{1\ max}$) level is applied to the input
- V_5 "OR" output voltage – logical "1" level output voltage when a logical "1" ($V_{1\ max}$) level is applied to the input
- V_6 Output latch voltage – input voltage to a flip-flop which causes the output voltage to change from a logical "1" level to a logical "0" level and corresponds to the point where the rate of change in the output voltage to the rate of the input voltage approaches infinity
- V_H Logical "1" input voltage
- V_L Logical "0" input voltage
- V_{OH} High-level output voltage when the saturated logic circuit output is in an "off" condition
- V_{OL} Low-level output voltage when the saturated logic output circuit is in an "on" condition
- ΔV_1, ΔV_5 Change in the "1" level output voltage as the load is varied from no load to full load

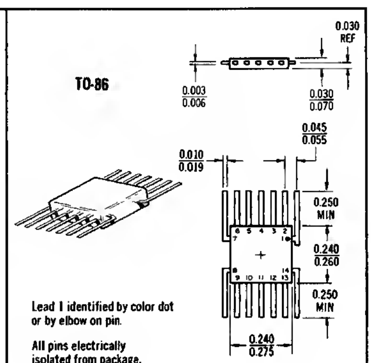
PACKAGES

All MECL integrated circuits are available in both the TO-91, 10-lead flat package and the 10-lead metal package. To order the flat package, add suffix "F" to basic type number; to order metal package, add suffix "G".

Exception: Type MC313F is available only in the TO-86, 14-lead flat package.



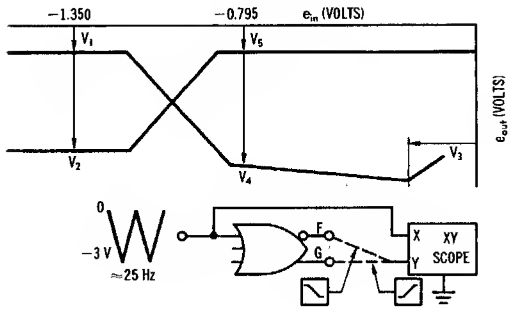


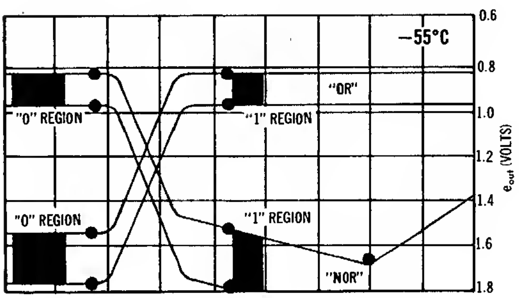


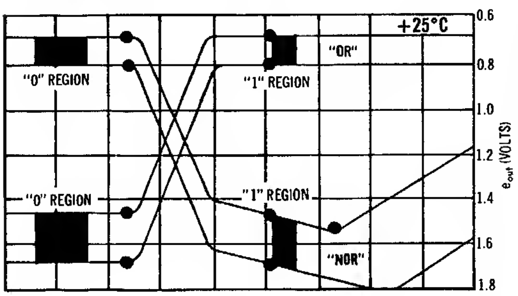
WORST-CASE TRANSFER CHARACTERISTICS

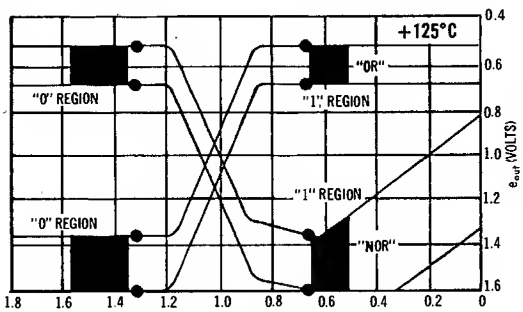
The following graphs show minimum and maximum limits of major parameters associated with the transfer characteristics of the MECL line. Min-Max limits, given at three different temperatures can be interpreted for design purposes as 10% to 90% spreads at all points on the curve except for guaranteed points in the Electrical Characteristics tables.

DEFINITIONS









MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0 Vdc)	V_{EE}	−10	Vdc
Base Input Voltage (V_{CC} = 0 Vdc)	V_{in}	0 Vdc to V_{EE}	Vdc
Output Source Current	I_O	20	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	−55 to +125	°C
AC Fan-In (Expandable Gates)	m	18	—
AC Fan-Out* (Gates and Flip-Flops)	n	15	—

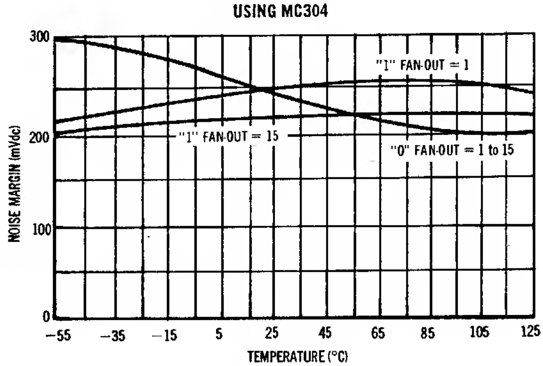
*Although a minimum dc fan-out of 25 is guaranteed in each electrical specification, it is recommended that the maximum ac fan-out of 15 be used for high-speed operation.

NOISE MARGINS (90 PERCENTILE)

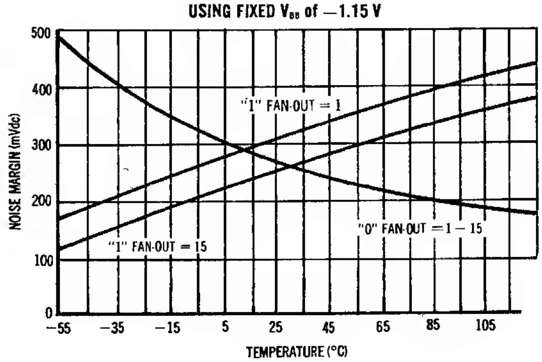
The following graphs show worst-case Noise Margins as a function of temperature and fan-out. Top graph illustrates the advantage gained through use of MC304 bias driver, as compared with non-compensated fixed bias source, bottom.

Note: Any unused input should be connected to V_{EE}.

USING MC304

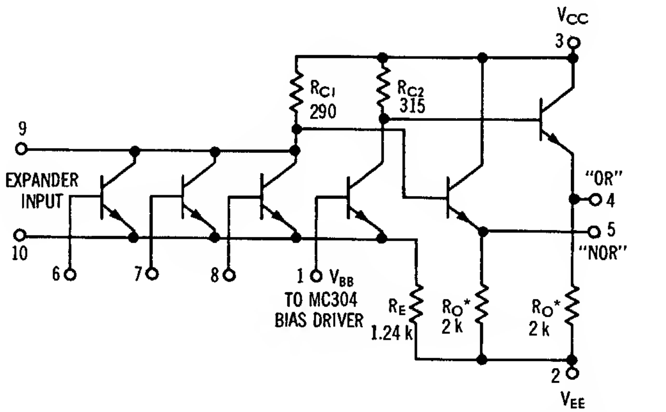


USING FIXED V_{BB} of −1.15 V



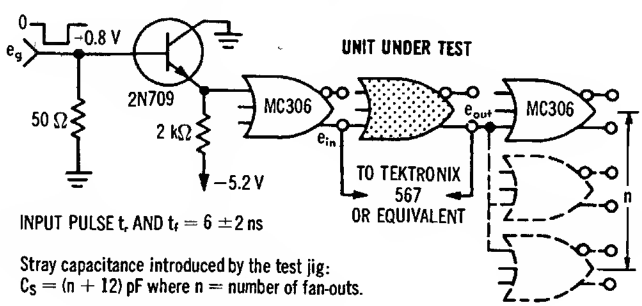
MC306 · MC307

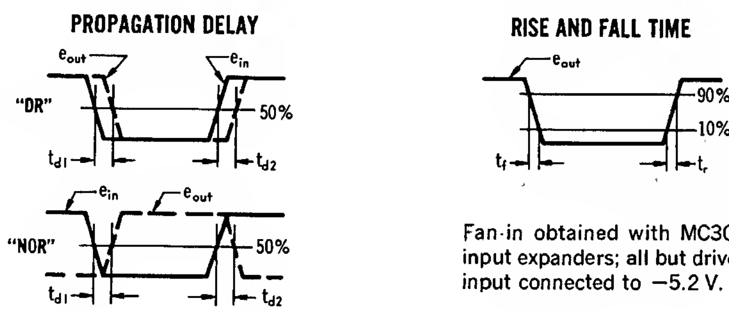
Expandable 3-input gates that provide the positive logic "NOR" function and its complement simultaneously. MC307 omits output pull-down resistors, permitting reduction of power dissipation.



*Resistors R_O are omitted in MC307 circuits to permit reduction of Power Dissipation in systems where logic operations are performed at circuit outputs.

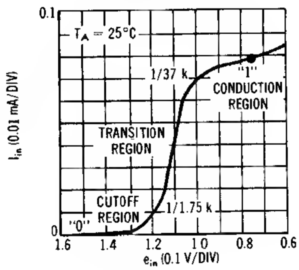
SWITCHING TIME TEST CIRCUIT



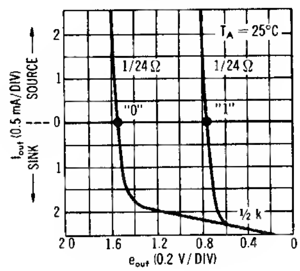


Fan-in obtained with MC305 input expanders; all but driven input connected to −5.2 V.

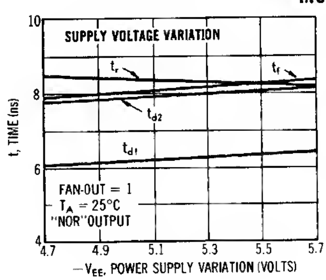
TYPICAL INPUT CHARACTERISTICS

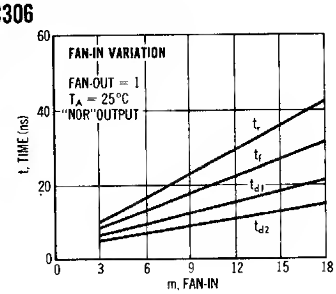


TYPICAL OUTPUT CHARACTERISTICS

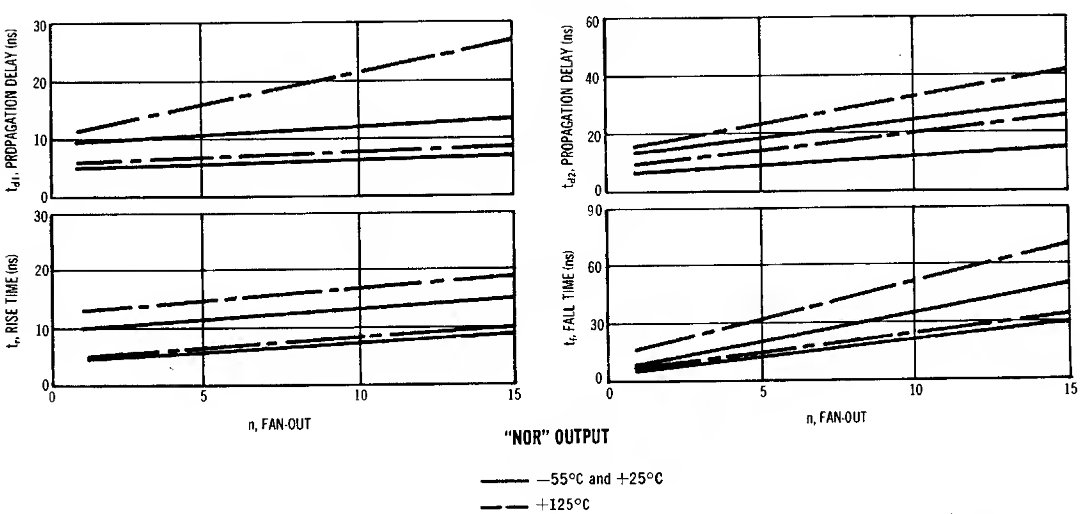


TYPICAL SWITCHING TIME VARIATIONS MC306





SWITCHING CHARACTERISTICS (10% to 90% distribution)



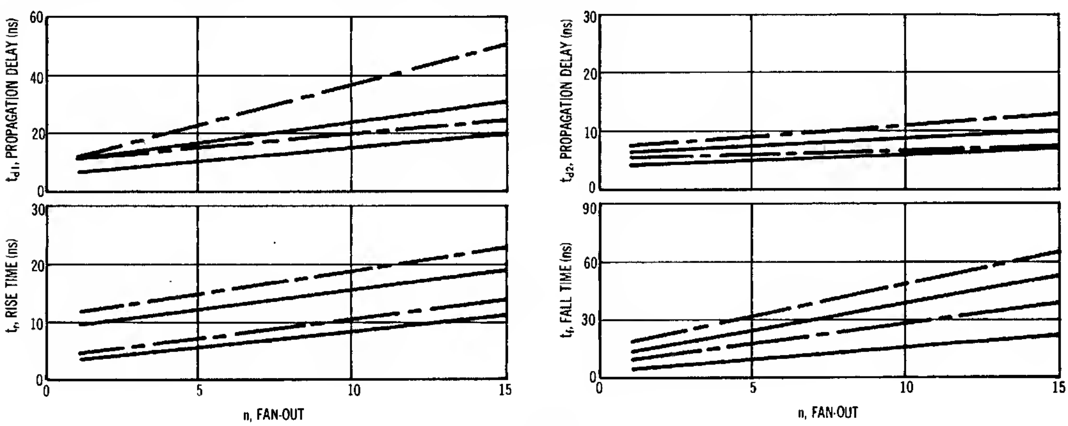
MC306, MC307 (continued)

ELECTRICAL CHARACTERISTICS

@ Test Temperature																
	Test Conditions Vdc ±1%															
−55°C	—	−0.945	−1.450	−5.20	−1.25											
+25°C	−0.690	−0.795	−1.350	−5.20	−1.15											
+125°C	—	−0.655	−1.300	−5.20	−1.00											
										Test Limits						
									Symbol	−55°C		+25°C		+125°C		
Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Pin No in ( )	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current MC306	—	—	—	2,6,7,8	1	—	—	3	I_E (2)	—	8.85	—	8.85	—	8.15	mAdc
MC307	—	—	—	2,6,7,8	1	—	—	3	I_E (2)	—	3.6	—	3.6	—	3.3	mAdc
Input Current	6	—	—	2,7,8	1	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,8,8	1	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8	1	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.855	Vdc
	—	—	7	2,6,8	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltagu	—	6	—	2,7,8	1	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	7	—	2,6,8	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,8,7	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "1" Output Voltagu	—	6	—	2,7,8	1	—	—	3	V_5 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	7	—	2,6,8	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,8,7	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "0" Output Voltage	—	—	6	2,7,8	1	—	—	3	V_2 (4)	−1.560	−1.850	−1.485	−1.750	−1.340	−1.675	Vdc
	—	—	7	2,8,8	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	—	8	2,7,8	1	—	5③	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"OR" Output Voltage Change (No load to full load)	—	6	—	2,7,8	1	—	4③	3	ΔV_5 (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8	1	8①	—	3	V_3 (5)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	2,6,8	1	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7	1	8①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	8	4	—	2,7,8	1	—	—	3	t_{d1} (4)	7.0	11.0	7.0	11.5	9.5	14.5	ns
	6	5	—	2,7,8	1	—	—	3	t_{d1} (5)	5.5	10.0	5.5	10.5	7.0	12.5	↓
	6	4	—	2,7,8	1	—	—	3	t_{d2} (4)	5.5	10.0	5.5	11.0	7.0	12.5	↓
	6	5	—	2,7,8	1	—	—	3	t_{d2} (5)	7.0	10.5	7.0	11.0	9.5	14.5	↓
Rise Time	6	4	—	2,7,8	1	—	—	3	t_r (4)	6.0	8.5	6.0	10.0	8.0	13.0	↓
	6	5	—	2,7,8	1	—	—	3	t_r (5)	7.5	11.5	7.5	12.5	9.5	15.0	↓
Fall Time	6	4	—	2,7,8	1	—	—	3	t_f (4)	6.5	10.5	6.5	12.0	9.0	15.0	↓
	6	5	—	2,7,8	1	—	—	3	t_f (5)	6.5	12.0	6.5	12.5	9.0	15.0	↓

Pins not listud are left opun. ① Input voltagu is adjusted to obtain dV "NOR / dV_{in} = 0. ③ Current test conditions: no load = 0; full load = −2.5mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



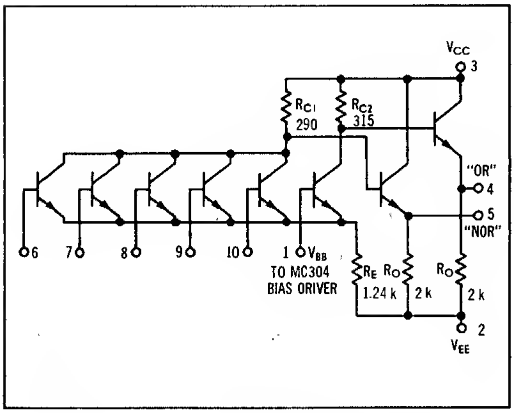
"OR" OUTPUT

——— −55°C and +25°C

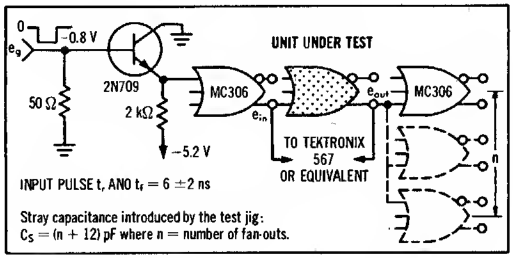
– – – +125°C

MC301

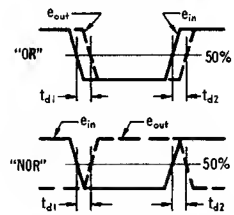
A 5-input gate that provides the positive logic "OR" function and its complement simultaneously.



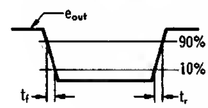
SWITCHING TIME TEST CIRCUIT



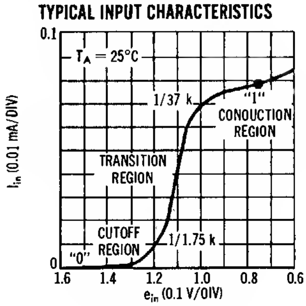
PROPAGATION DELAY



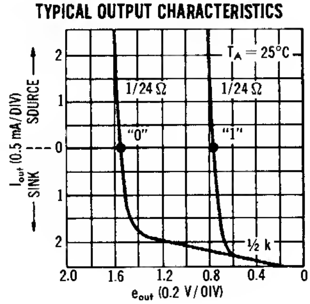
RISE AND FALL TIME



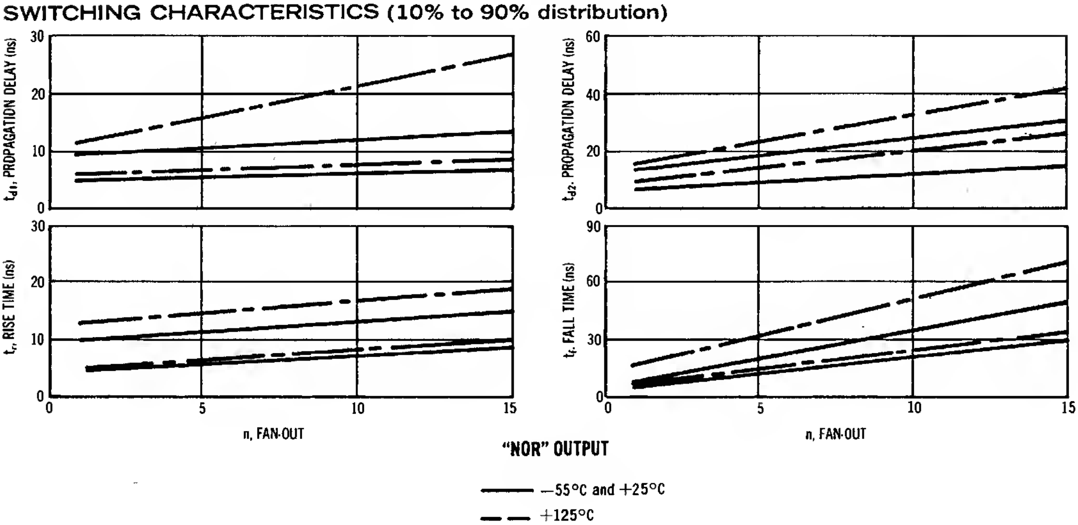
TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



SWITCHING CHARACTERISTICS (10% to 90% distribution)

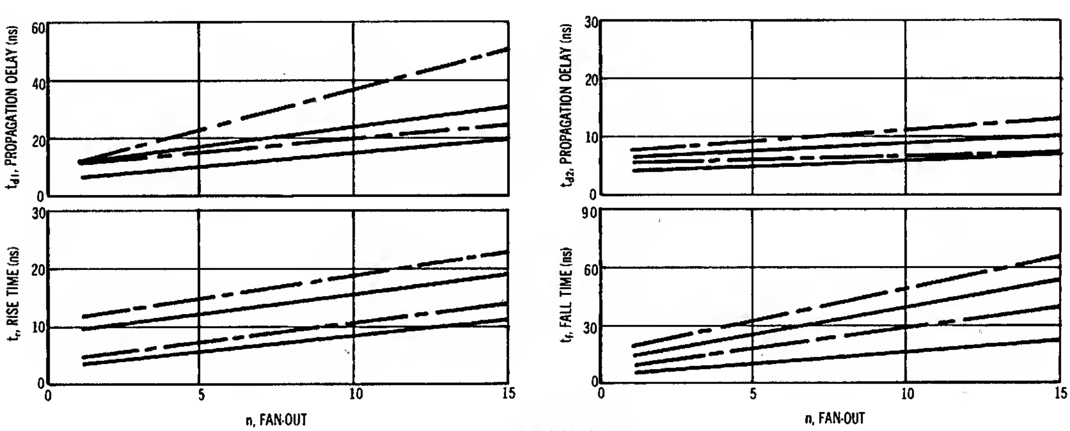


ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%				
−55°C	—	−0.945	−1.450	−5.20	−1.25
+25°C	−0.690	−0.795	−1.350	−5.20	−1.15
+125°C	—	−0.655	−1.300	−5.20	−1.00

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	−55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	2,6,7,8,9,10	1	—	—	3	I_E (2)	—	8.85	—	8.85	—	8.15	mAdc
Input Current	6	—	—	2,7,8,9,10	1	—	—	3	I_{in} (6)	—	—	—	100	—	—	µAdc
	7	—	—	2,6,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	a	—	—	2,6,7,9,10	1	—	—	3	I_{in} (8)	—	—	—		—	—	
	9	—	—	2,6,7,8,10	1	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,6,7,8,9	1	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8,9,10	1	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7	2,6,8,9,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7,9,10	1	—	—	3	V_1 (5)							
	—	—	9	2,8,7,8,10	1	—	—	3	V_1 (5)							
	—	—	10	2,6,7,8,9	1	—	—	3	V_1 (5)							
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8,9,10	1	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	7	—	2,6,8,9.10	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,8,7,9,10	1	—	—	3	V_4 (5)							
	—	9	—	2,6,7,8,10	1	—	—	3	V_4 (5)							
	—	10	—	2,6,7,8,9	1	—	—	3	V_4 (5)							
"OR" Logical "1" Output Voltage	—	6	—	2,7,8,9,10	1	—	—	3	V_5 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.855	Vdc
	—	7	—	2,6,8,9,10	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7,9,10	1	—	—	3	V_5 (4)							
	—	9	—	2,6,7,8,10	1	—	—	3	V_5 (4)							
	—	10	—	2,6,7,8,9	1	—	—	3	V_5 (4)							
"OR" Logical "0" Output Voltage	—	—	6	2,7,8,9,10	1	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	—	7	2,6,8,9,10	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7,9.10	1	—	—	3	V_2 (4)							
	—	—	9	2,6,7,8,10	1	—	—	3	V_2 (4)							
	—	—	10	2,6,7,8,9	1	—	—	3	V_2 (4)							
"NOR" Output Voltage Change (No load to full load)	—	—	6	2,7,8,9,10	1	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"OR" Output Voltage Change (No load to full load)	—	6	—	2,7,8,9,10	1	—	4②	3	ΔV_5 (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8,9,10	1	6①	—	3	V_3 (5)	—	−0.40	—	−0.55	—	−0.88	Vdc
	—	—	—	2,6,8,9,10	1	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,9,10	1	8①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,6,7,8,10	1	9①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,8,7,8,9	1	10①	—	3	V_3 (5)	—		—		—		
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	4	—	2,7,8,9,10	1	—	—	3	t_{d1} (4)	8.0	12.0	8.5	12.5	10.0	15.5	ns
	6	5	—	2,7,8,9,10	1	—	—	3	t_{d1} (5)	6.5	10.0	8.5	11.0	7.5	14.0	↓
	8	4	—	2,7,8,9,10	1	—	—	3	t_{d2} (4)	5.5	9.0	6.0	10.0	8.0	12.0	
	6	5	—	2,7,8,9,10	1	—	—	3	t_{d2} (5)	7.5	11.0	8.0	12.5	10.0	15.5	
Rise Time	6	4	—	2,7,8,9,10	1	—	—	3	t_r (4)	6.5	9.0	7.0	10.0	10.5	15.5	
	6	5	—	2,7,8,9,10	1	—	—	3	t_r (5)	8.5	14.0	9.0	14.5	11.0	17.5	
Fall Time	8	4	—	2,7,8,9,10	1	—	—	3	t_f (4)	7.0	11.5	7.5	13.0	10.0	16.0	
	8	5	—	2,7,8,9,10	1	—	—	3	t_f (5)	7.0	12.0	7.5	12.5	10.0	15.5	

Pins not listed are left open ① Input voltage is adjusted to obtain dV "NOR / dV_{in} = "0". ② Current test conditions: no load = 0; full load = −2.5mAdc ±5%.



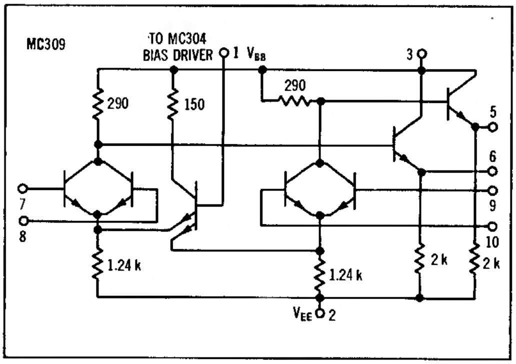
"OR" OUTPUT

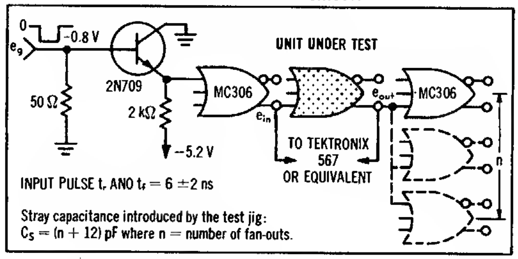
—— −55°C and +25°C

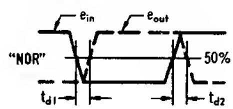
– – – +125°C

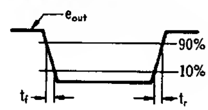
MC309 · MC310 · MC311

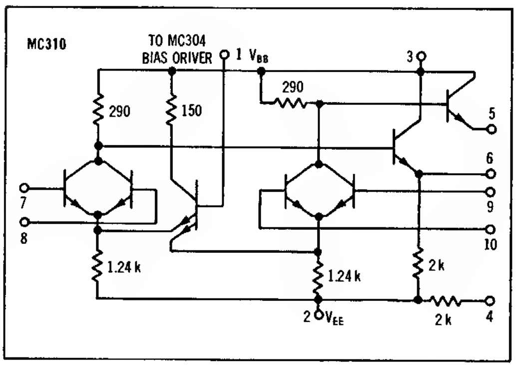
Dual 2-input gates that provide the positive logic "NOR" function. MC309 has two output pull-down resistors; MC310 has one of the output pull-down resistors optional; MC311 omits one output pull-down resistor and has the second optional.

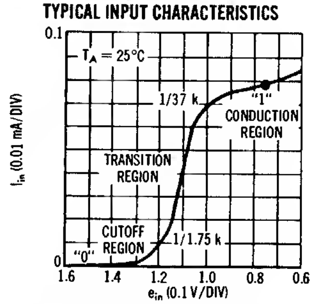


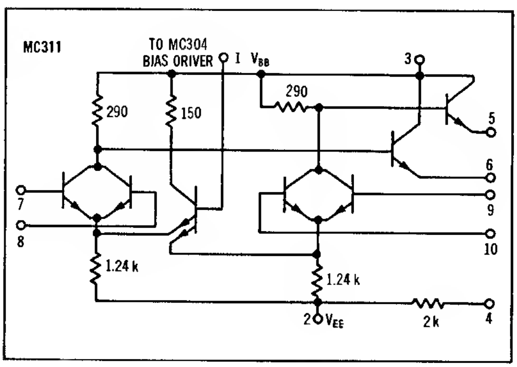


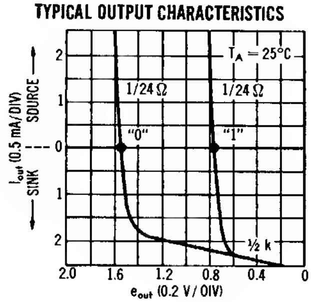












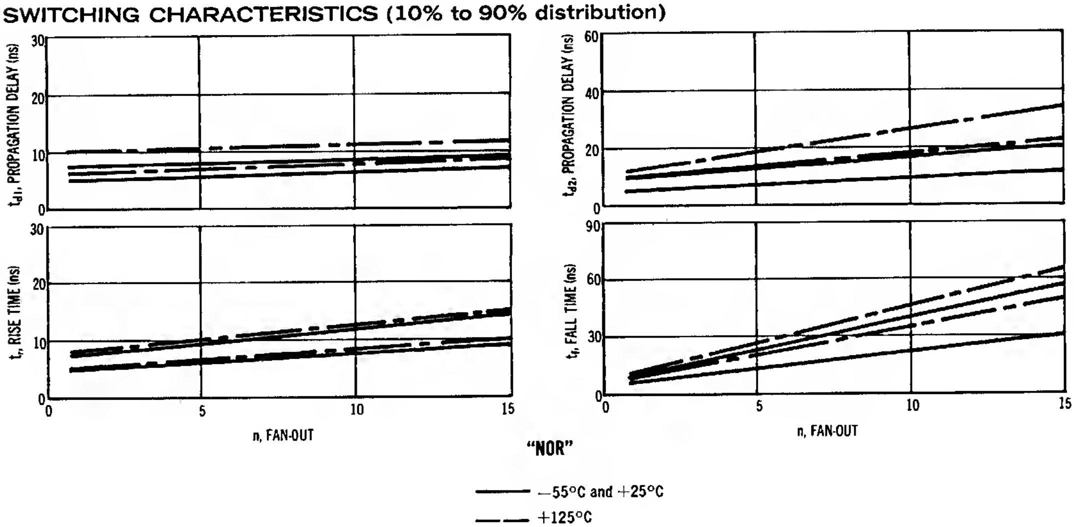
ELECTRICAL CHARACTERISTICS

@ Test Temperature	V_H	$V_{I\,max}$	V_L	V_{EE}	V_{BB}
	Test Conditions Vdc ±1%				
−55°C	—	−0.945	−1.450	−5.20	−1.25
+25°C	−0.690	−0.795	−1.350	−5.20	−1.15
+125°C	—	−0.655	−1.300	−5.20	−1.00

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current MC309, MC310	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	13.0	—	13.0	—	12.0	mAdc
MC311	—	—	—	2,7,6,9,10	1	—	—	3	I_E (2)	—	10.1	—	10.1	—	9.3	mAdc
Input Current	7	—	—	2,6,9,10	1	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	6	—	—	2,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,7,8,10	1	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	2,7,6,9	1	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	7	2,6,9,10	1	—	—	3	V_1 (6)	−0.625	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	6	2,7,9,10	1	—	—	3	V_1 (6)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,7,8,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	2,7,6,9	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	7	—	2,8,9,10	1	—	—	3	V_4 (6)	−1.560	−1.650	−1.465	−1.750	−1.340	−1.675	Vdc
	—	6	—	2,7,9,10	1	—	—	3	V_4 (6)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,7,8,10	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	2,7,8,9	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	—	—	2,7,8,9,10	1	—	6②	3	ΔV_1 (6)	—	−0.055	—	−0.055	—	−0.060	Vdc
	—	—	—	2,7,8,9,10	1	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Vdc
"NOR" Saturation Breakpoint Voltage	—	—	—	2,6,9,10	1	7①	—	3	V_3 (6)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	2,7,9,10	1	6①	—	3	V_3 (6)	—	↓	—	↓	—	↓	↓
	—	—	—	2,7,8,10	1	9①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,7,6,9	1	10①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	7	6	—	2,8,9,10	1	—	—	3	t_{d1} (6)	5.5	10.0	6.0	11.0	7.0	12.0	ns
	10	5	—	2,7,6,9	1	—	—	3	t_{d1} (5)	5.5	10.0	6.0	11.0	7.0	12.0	↓
	7	6	—	2,6,9,10	1	—	—	3	t_{d2} (6)	6.5	13.0	7.0	13.5	9.5	15.0	↓
	10	5	—	2,7,6,9	1	—	—	3	t_{d2} (5)	6.5	13.0	7.0	13.5	9.5	15.0	↓
Rise Time	7	6	—	2,8,9,10	1	—	—	3	t_r (6)	6.0	12.0	6.0	12.0	7.0	13.5	↓
	10	5	—	2,7,6,9	1	—	—	3	t_r (5)	6.0	12.0	6.0	12.0	7.0	13.5	↓
Fall Time	7	6	—	2,6,9,10	1	—	—	3	t_f (6)	7.0	13.0	7.5	14.0	9.5	17.0	↓
	10	5	—	2,7,6,9	1	—	—	3	t_f (5)	7.0	13.0	7.5	14.0	9.5	17.0	↓

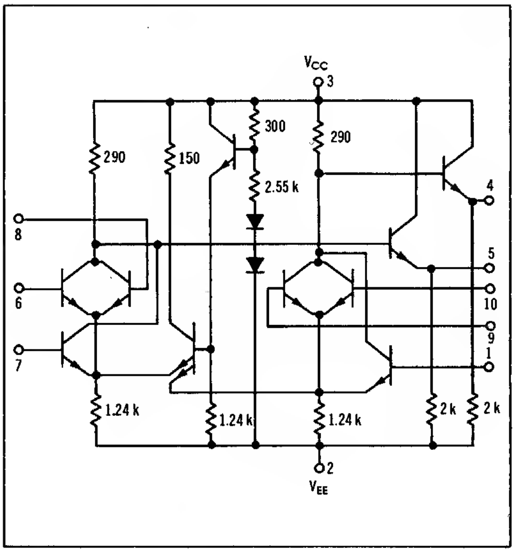
Pins not listed are left open For MC310, connect pin 4 to pin 5 for all tests ① Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0.
② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

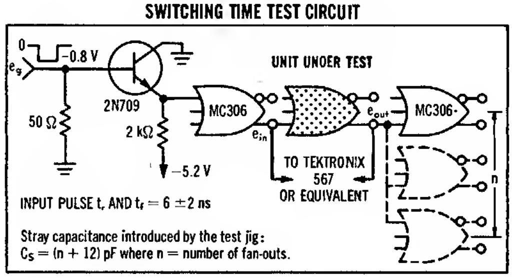


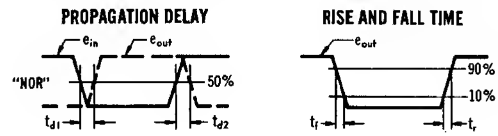
MC312A

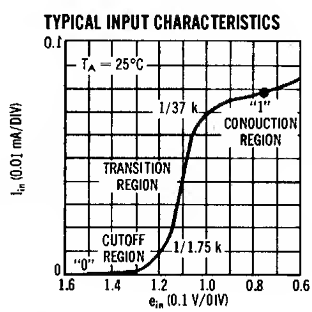
Dual 3-input gate that provides the positive logic "NOR" function, and features an internal bias driver. This gate is available without bias driver as MC312.

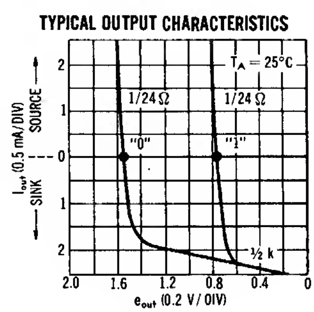


SWITCHING TIME TEST CIRCUIT









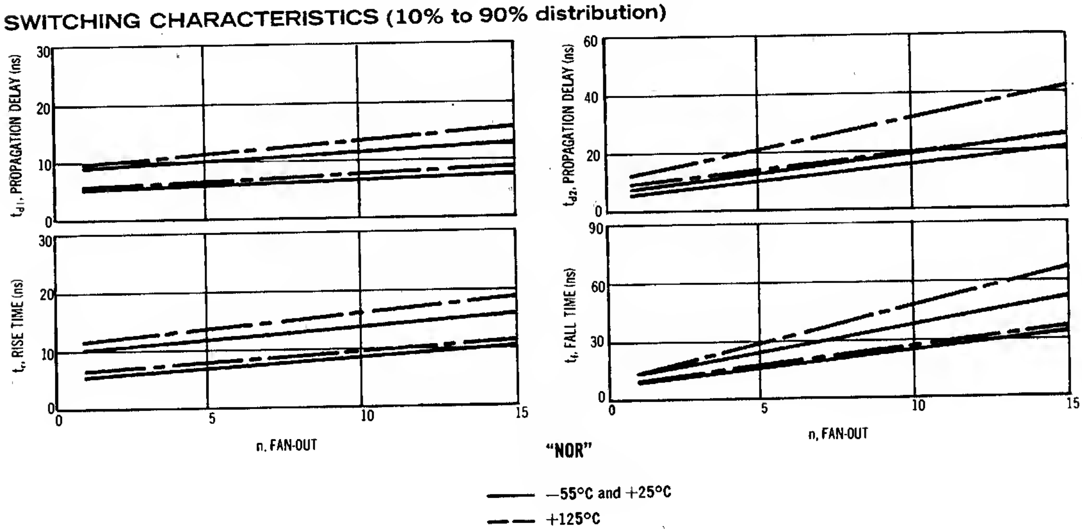
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
−55°C	—	−0.945	−1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	1,2,6,7,8,9,10	—	—	3	I_E (2)	—	17.7	—	17.0	—	16.4	mAdc
Input Current	1	—	—	2,6,7,8,9,10	—	—	3	I_{in} (1)	—	—	—	100	—	—	µAdc
	6	—	—	1,2,7,8,9,10	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	6	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7	1,2,6,8,9,10	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	1,2,6,7,9,10	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	1	2,6,7,8,9,10	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	1,2,6,7,8,10	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	1,2,6,7,8,9	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	6	—	1,2,7,8,9,10	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	7	—	1,2,6,8,9,10	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	1,2,6,7,9,10	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	1	—	2,6,7,8,9,10	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	1,2,6,7,8,10	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	1,2,6,7,8,9	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change	—	—	6	1,2,7,8,9,10	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Volts
	—	—	1	2,6,7,8,9,10	—	4②	3	ΔV_1 (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	1,2,6,8,9,10	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,9,10	8①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,8,10	9①	—	3	V_3 (4)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,8,9	10①	—	3	V_3 (4)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	1,2,7,8,9,10	—	—	3	t_{d1} (5)	6.5	10.5	6.5	10.5	7.5	11.5	ns
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d1} (4)	6.5	10.5	6.5	10.5	7.5	11.5	↓
	6	5	—	1,2,7,8,9,10	—	—	3	t_{d2} (5)	8.5	11.5	8.5	11.5	10.0	15.0	↓
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d2} (4)	8.5	11.5	8.5	11.5	10.0	15.0	↓
Rise Time	6	5	—	1,2,7,8,9,10	—	—	3	t_r (5)	9.0	12.5	9.5	12.5	11.5	15.5	↓
	1	4	—	2,6,7,8,9,10	—	—	3	t_r (4)	9.0	12.5	9.5	12.5	11.5	15.5	↓
Fall Time	6	5	—	1,2,7,8,9,10	—	—	3	t_f (5)	8.5	14.0	9.0	14.0	11.5	17.0	↓
	1	4	—	2,6,7,8,9,10	—	—	3	t_f (4)	8.5	14.0	9.0	14.0	11.5	17.0	↓

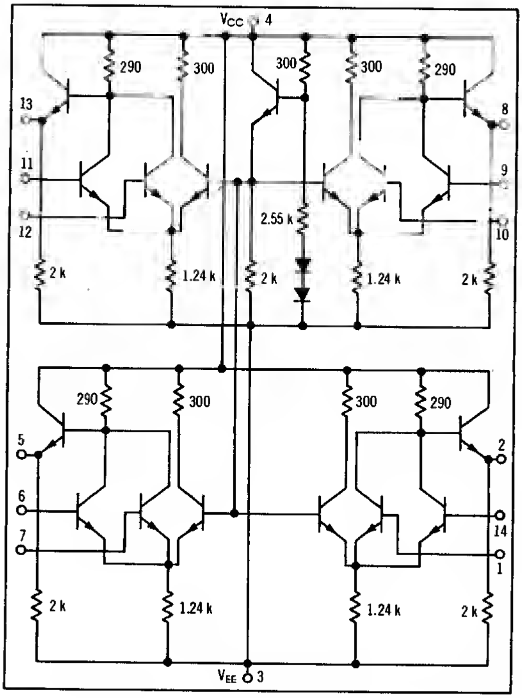
Pins not listed are left open.
① Input voltage is adjusted to obtain dv "NOR"/dV_{in} = 0. ② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

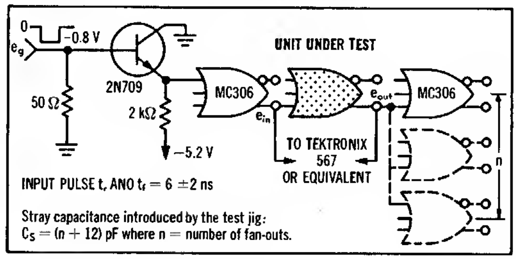


MC313F

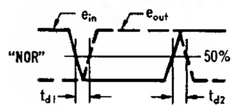
Quad 2-input gate that provides the positive logic "NOR" function, and features an internal bias driver.



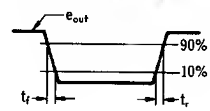
SWITCHING TIME TEST CIRCUIT



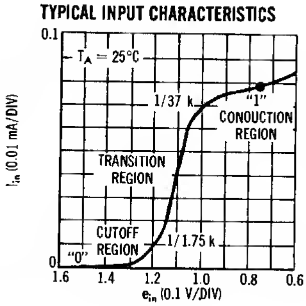
PROPAGATION DELAY



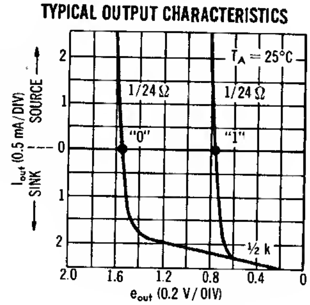
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



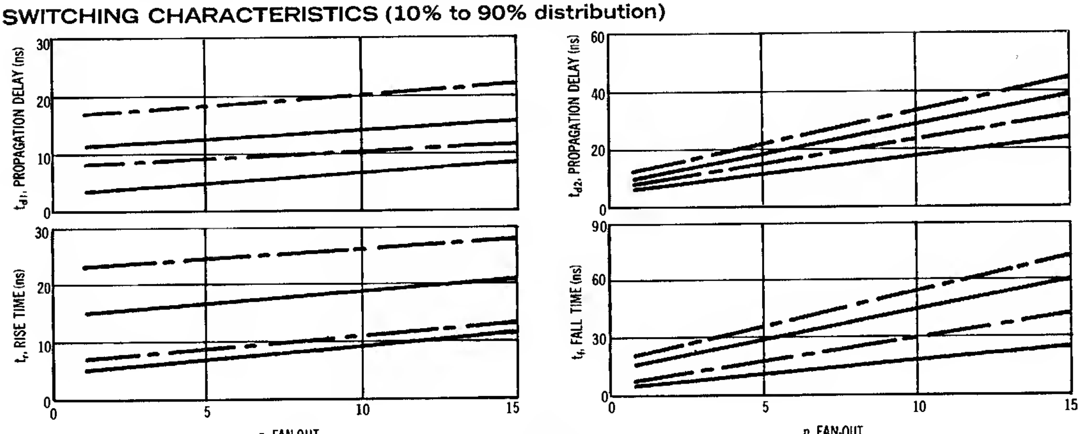
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ± 1%			
	V_H	$V_{I\,max}$	V_L	V_{EE}
−55°C	—	−0.945	−1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	1,3,6,7,9,10,11,12,14	—	—	4	I_E (3)	—	31.0	—	30.0	—	29.0	mAdc
Input Current	1	—	—	3,6,7,9,10,11,12,14	—	—	4	I_{in} (1)	—	—	—	100	—	—	µAdc
	6	—	—	1,3,7,9,10,11,12,14	—	—	4	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,3,6,9,10,11,12,14	—	—	4	I_{in} (7)	—	—	—	↓	—	—	↓
	9	—	—	1,3,6,7,10,11,12,14	—	—	4	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	1,3,6.7,9,11,12,14	—	—	4	I_{in} (10)	—	—	—	↓	—	—	↓
	11	—	—	1,3,6,7,9,10,12,14	—	—	4	I_{in} (11)	—	—	—	↓	—	—	↓
	12	—	—	1,3,6,7,9,10,11,14	—	—	4	I_{in} (12)	—	—	—	↓	—	—	↓
	14	—	—	1,3,6,7,9,10,11,12	—	—	4	I_{in} (14)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	1	3,6,7,9,10,11,12,14	—	—	4	V_1 (2)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	6	1,3,7,9,10,11,12,14	—	—	4	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	7	1,3,6.9,10,11,12,14	—	—	4	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	1,3,6,7,10,11,12,14	—	—	4	V_1 (8)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	1,3,6,7,9,11,12,14	—	—	4	V_1 (8)	↓	↓	↓	↓	↓	↓	↓
	—	—	11	1,3,6,7,9,10,12,14	—	—	4	V_1 (13)	↓	↓	↓	↓	↓	↓	↓
	—	—	12	1,3,6,7,9,10,11,14	—	—	4	V_1 (13)	↓	↓	↓	↓	↓	↓	↓
	—	—	14	1,3,6,7,9,10,11,12	—	—	4	V_1 (2)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	1	—	3,6,7,9,10,11,12,14	—	—	4	V_4 (2)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	6	—	1,3,7,9,10,11,12,14	—	—	4	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	7	—	1,3,6,9,10,11,12,14	—	—	4	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	1,3 6,7,10,11,12,14	—	—	4	V_4 (8)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	1,3,6,7,9,11,12,14	—	—	4	V_4 (8)	↓	↓	↓	↓	↓	↓	↓
	—	11	—	1,3,6,7,9,10,12,14	—	—	4	V_4 (13)	↓	↓	↓	↓	↓	↓	↓
	—	12	—	1,3,6,7,9,10,11,14	—	—	4	V_4 (13)	↓	↓	↓	↓	↓	↓	↓
	—	14	—	1,3,6,7,9,10,11,12	—	—	4	V_4 (2)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	—	—	1,3,6,7,9,10,11,12,14	—	2②	4	ΔV_1 (2)	—	−0.055	—	−0.055	—	−0.060	Volts
	—	—	—	1,3,6,7,9,10,11,12,14	—	5②	4	ΔV_1 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	—	8②	4	ΔV_1 (8)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	—	13②	4	ΔV_1 (13)	—	↓	—	↓	—	↓	↓
"NOR" Saturation Breakpoint Voltage	—	—	—	1,3,6,7,9,10,11,12,14	1①	—	4	V_3 (2)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	1,3,6,7,9,10,11,12,14	7①	—	4	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	10①	—	4	V_3 (8)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	12①	—	4	V_3 (13)	—	↓	—	↓	—	↓	↓
	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Switching Time Propagation Delay Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_{d1} (2)	6.5	11.0	6.5	11.0	8.0	14.5	ns
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_{d1} (5)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	1,3,6,7,10,11,12.14	—	—	4	t_{d1} (8)	↓	↓	↓	↓	↓	↓	↓
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_{d1} (13)	↓	↓	↓	↓	↓	↓	↓
	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_{d2} (2)	8.5	13.5	8.5	13.5	10.0	16.0	↓
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_{d2} (5)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_{d2} (8)	↓	↓	↓	↓	↓	↓	↓
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_{d2} (13)	↓	↓	↓	↓	↓	↓	↓
Rise Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_r (2)	8.5	12.5	9.0	12.5	11.0	15.5	↓
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_r (5)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	1,3,6,7.10,11,12,14	—	—	4	t_r (8)	↓	↓	↓	↓	↓	↓	↓
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_r (13)	↓	↓	↓	↓	↓	↓	↓
Fall Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_f (2)	9.0	14.0	9.5	14.0	11.5	17.0	↓
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_f (5)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_f (8)	↓	↓	↓	↓	↓	↓	↓
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_f (13)	↓	↓	↓	↓	↓	↓	↓

Pins not listed are left open ① Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0. ② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



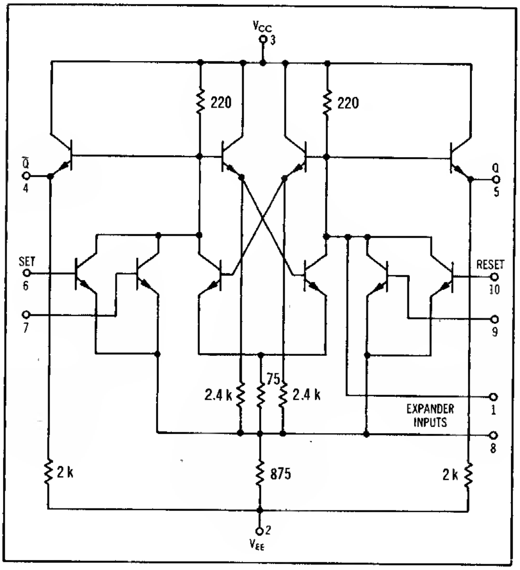
"NOR"

——— −55°C and +25°C

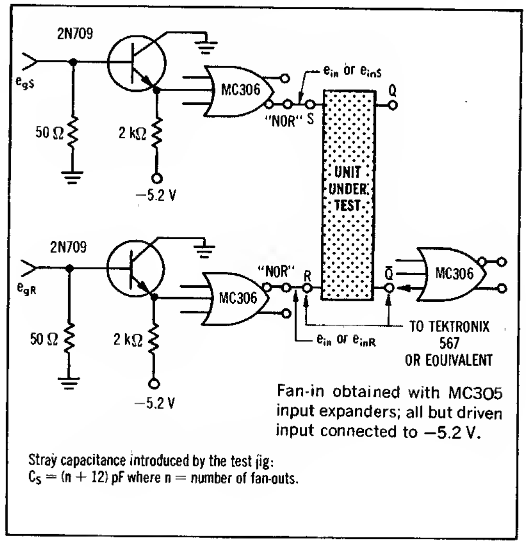
— — — +125°C

MC302

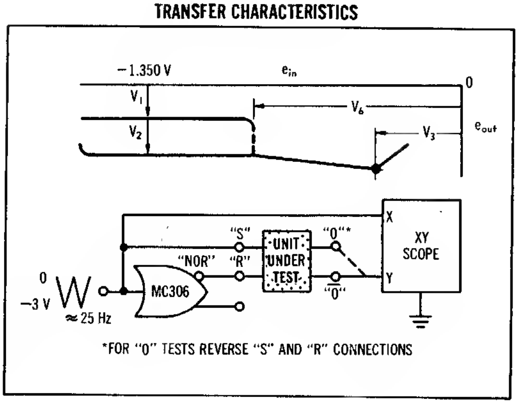
DC Set-Reset flip-flop with an expandable input and buffered outputs.



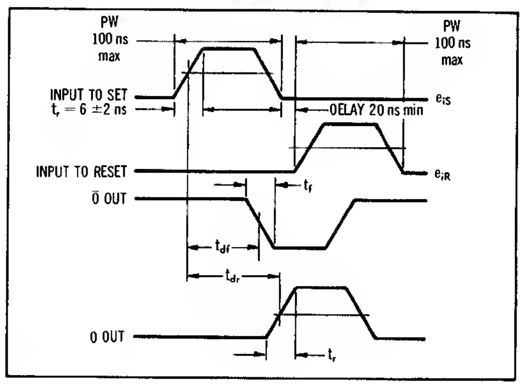
SWITCHING TIME TEST CIRCUIT



TRANSFER CHARACTERISTICS



SWITCHING TIME WAVEFORMS

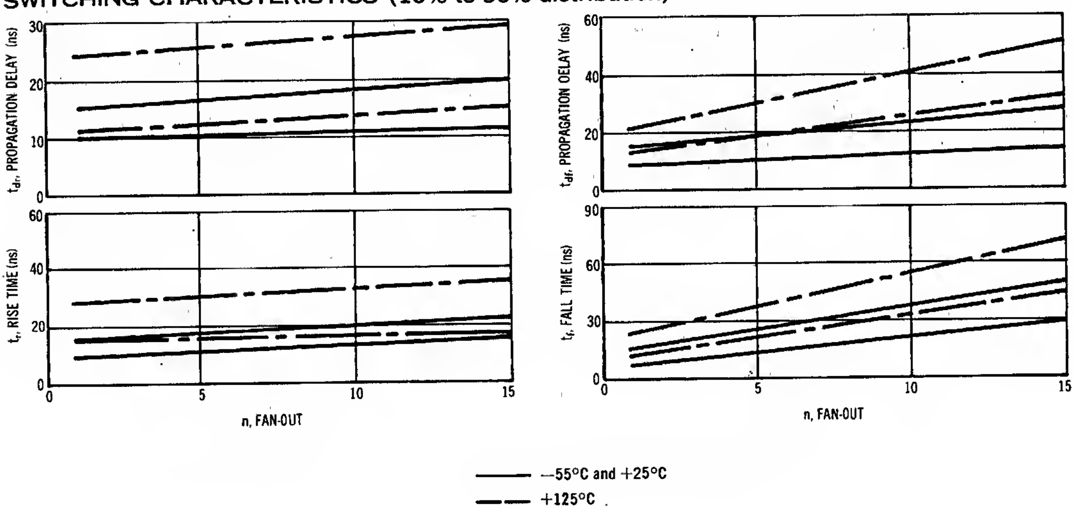


ELECTRICAL CHARACTERISTICS

Characteristic	V_{IH} Pin No	$V_{IL\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Test Conditions Vdc ±1% @ Test Temperature −55°C	—	−0.945	−1.450	−5.20											
+25°C	−0.690	−0.795	−1.350	−5.20											
+125°C	—	−0.655	−1.300	−5.20											
Power Supply Drain Current	—	—	—	2,6,7,9,10	—	—	3	I_E (6)	—	10.35	—	10.35	—	9.52	mAdc
Input Current	6	—	—	2,7,9,10	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,9,10	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	9	—	—	2,6,7,10	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	2,6,7,9	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"Q" Logical "1" Output Voltage	—	—	6③	2,7,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7③	2,6,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"Q" Logical "0" Output Voltage	—	—	9③	2,6,7,10	—	—	3	V_2 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	—	10③	2,6,7,9	—	—	3	V_2 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"$\overline{Q}$" Logical "1" Output Voltage	—	—	9③	2,6,7,10	—	—	3	V_1 (4)	−0.625	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	10③	2,6,7,9	—	—	3	V_1 (4)	−0.625	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"$\overline{Q}$" Logical "0" Output Voltage	—	—	6③	2,7,9,10	—	—	3	V_2 (4)	−1.560	−1.650	−1.465	−1.750	−1.340	−1.675	Vdc
	—	—	7③	2,6,9,10	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"Q" Output Voltage Change	—	6	—	2,7,9,10	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"$\overline{Q}$" Output Voltage Change	—	10	—	2,6,7,9	—	4②	3	ΔV_1 (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	2,7,9	6,10①	—	3	V_3 (5)	—	−0.50	—	−0.65	—	−0.75	Vdc
"$\overline{Q}$" Saturation Breakpoint Voltage	—	—	—	2,7,9	6,10①	—	3	V_3 (4)	—	−0.50	—	−0.65	—	−0.75	Vdc
"Q" or "$\overline{Q}$" Latch Voltage	—	—	—	2,7,9	6,10④	—	3	V_4 (6,10)	−1.16	−1.34	−1.09	−1.21	−0.93	−1.07	Vdc
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6,10	4,5	—	2,7,9	—	—	3	t_{dr} (4,5)	9.0	14.0	10.5	16.0	22.0	29.0	ns
	6,10	4,5	—	2,7,9	—	—	3	t_{df} (4,5)	8.5	14.0	11.5	19.5	16.0	24.0	↓
Rise Time	6,10	4,5	—	2,7,9	—	—	3	t_r (4,5)	9.0	15.0	11.5	19.0	23.0	31.0	↓
Fall Time	6,10	4,5	—	2,7,9	—	—	3	t_f (4,5)	7.0	13.0	12.5	19.5	18.0	29.0	↓

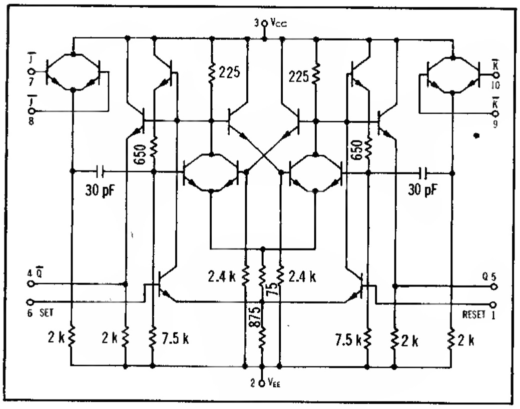
Pins not listed are left open. ① Input voltage is adjusted to obtain dV "$\overline{Q}$" / dV_{in} = 0; dV "Q" / dV_{in} = 0. ② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%. ③ Apply momentary $V_{IL\,max}$ to set output, then V_L for measurement. ④ Input voltage is adjusted to obtain $dV_1 / dV_{in} \approx \infty$.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

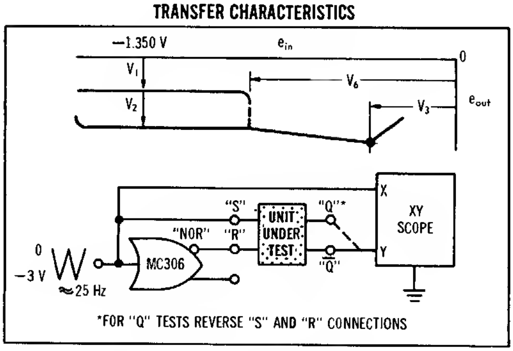


MC308

AC-coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.



TRANSFER CHARACTERISTICS



*FOR "Q" TESTS REVERSE "S" AND "R" CONNECTIONS

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

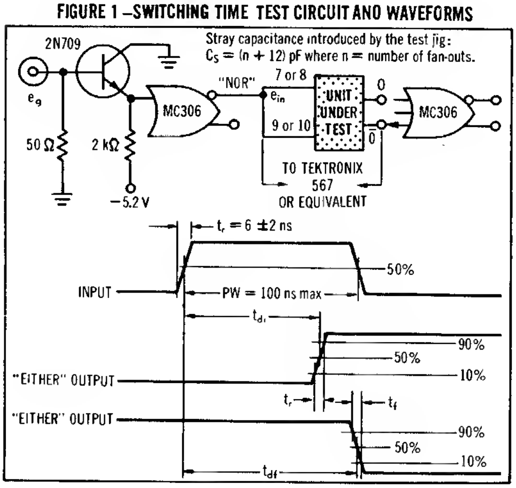


FIGURE 2 – INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

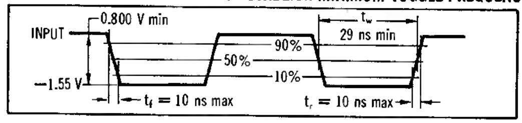


FIGURE 3 – SENSITIVITY (NO TOGGLE)

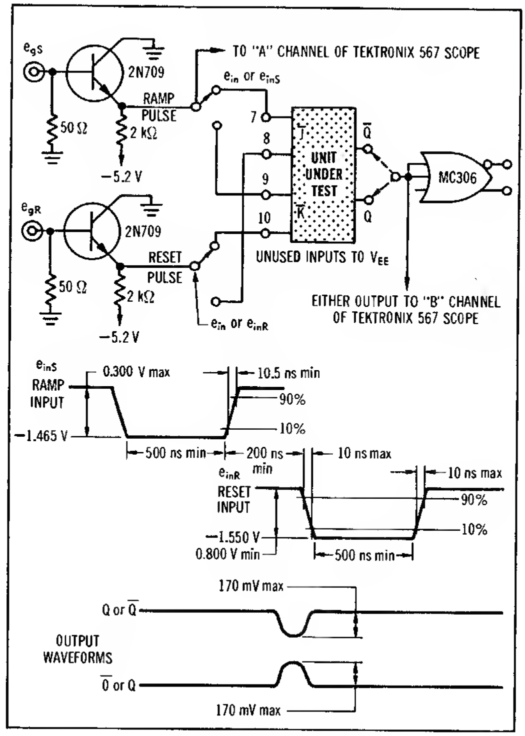
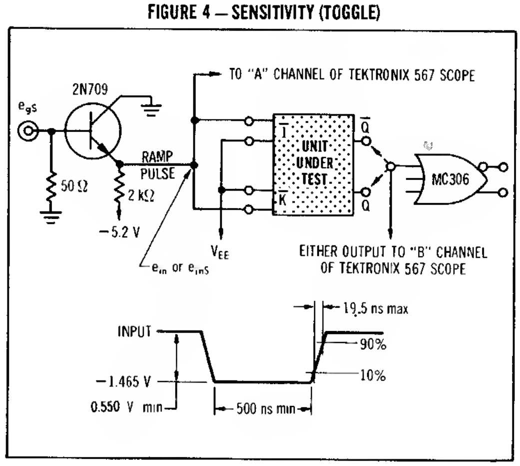


FIGURE 4 – SENSITIVITY (TOGGLE)

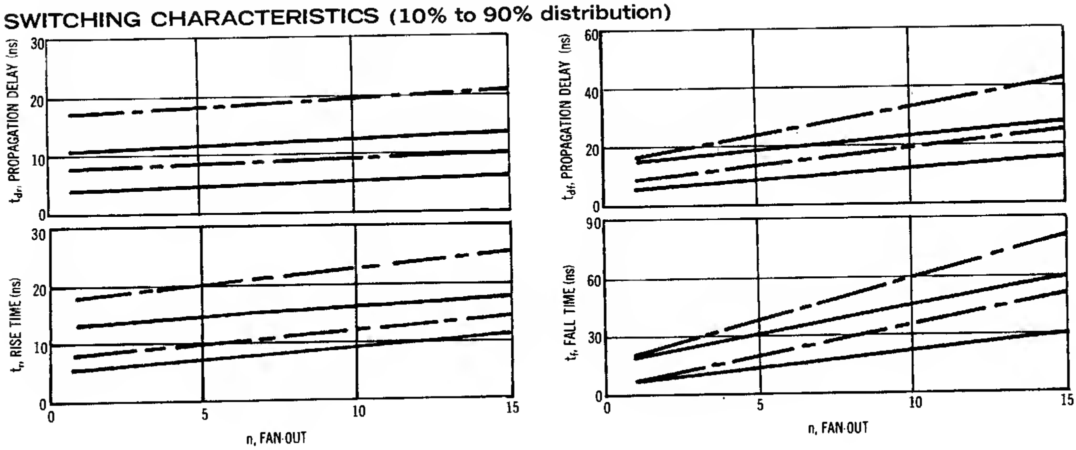


ELECTRICAL CHARACTERISTICS

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	−55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Test Conditions Vdc ±1% @ Test Temperature −55°C	—	−0.945	−1.450	−5.20											
+25°C	−0.690	−0.795	−1.350	−5.20											
+125°C	—	−0.655	−1.300	−5.20											
Power Supply Drain Current	—	7,10	—	1,2,6,8,9	—	—	3	I_E (2)	—	22.0	—	21.0	—	19.5	mAdc
Input Current	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	100	—	—	µAdc
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—		—	—	
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"Q" Logical "0" Output Voltage	—	—	1③	2,6,7,8,9,10	—	—	3	V_2 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"$\overline{Q}$" Logical "1" Output Voltage	—	—	1③	2,6,7,0,9,10	—	—	3	V_1 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"$\overline{Q}$" Logical "0" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"Q" Output Voltage Change	—	6	—	1,2,7,8,9,10	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"$\overline{Q}$" Output Voltage Change	—	1	—	2,6,7,8,9,10	—	4②	3	ΔV_1 (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9.10	6①	—	3	V_3 (5)	—	−0.50	—	−0.65	—	−0.75	Vdc
"$\overline{Q}$" Saturation Breakpoint Voltage	—	—	—	2,6,7,0,9,10	1①	—	3	V_3 (4)	—	−0.50	—	−0.65	—	−0.75	Vdc
"Q" or "$\overline{Q}$" Latch Voltage	—	—	—	2,7,8,9,10	1,6④	—	3	V_6 (1,6)	−1.16	−1.34	−1.09	−1.21	−0.93	−1.07	Vdc
	Pulse In	Pulse Out													
Toggle Froquency (See Figures 1 and 2)	7,10	5		1,2,6,9	—	—	3	f_{Tog}	—	—	15	—	—	—	MHz
Sensitivity (No Toggle)	7,10	4		1,2,6,0.9	—	—	3	See Figure 3							
	8,9	5		1,2,6,7,10	—	—	3	See Figure 3							
Sensitivity (Toggle)	7,10	4,5		1,2,6,8,9	—	—	3	See Figure 4							
									Typ	Max	Typ	Max	Typ	Max	
Switching Times Propagation Oelay	7,10	4,5		1,2,6,0,9	—	—	3	t_{dr} (4,5)	7.0	11.5	7.0	12.5	9.5	18.5	ns
	7,10	4,5		1,2,6,8,9	—	—	3	t_{df} (4,5)	8.5	14.0	8.5	14.5	10.0	16.5	
Riso Time	7,10	4,5		1,2,6,8,9	—	—	3	t_r (4,5)	6.5	13.0	6.5	13.0	10.0	18.5	
Fall Time	7,10	4,5		1,2,6,8,9	—	—	3	t_f (4,5)	7.5	14.5	0.5	15.5	11.5	20.0	

Pins not listed are left open. ① Input voltage is adjusted to obtain $dV_{out}/dV_{in} = 0$. ② Current test conditions: no load = 0 to full load = −2.5 mAdc ±5%.
③ Apply momentary $V_{I\,max}$ to set output, then V_{in} for measurement. ④ Input voltage is adjusted to obtain $dV_1/dV_{in} = \infty$.

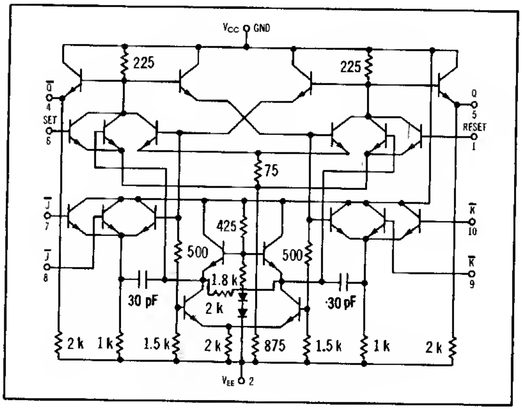
SWITCHING CHARACTERISTICS (10% to 90% distribution)



——— −55°C and +25°C
— — — +125°C

MC314

High-speed ac-coupled J-K flip-flop with dc Set and Reset input for counter and shift register applications up to 30 MHz operation.



TRANSFER CHARACTERISTICS

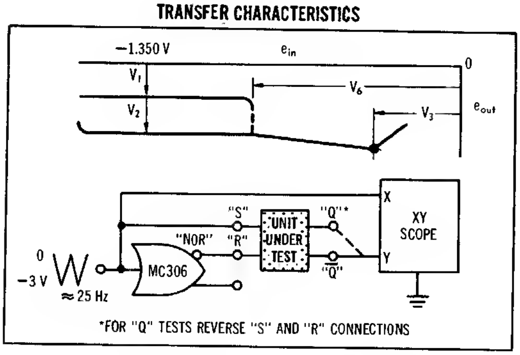


FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

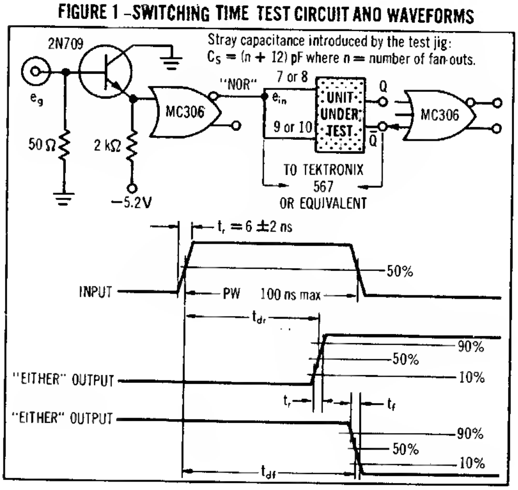


FIGURE 2 – INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

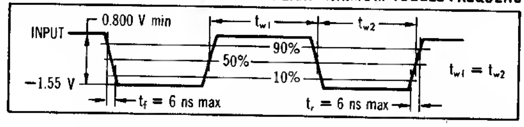


FIGURE 3 – SENSITIVITY (NO TOGGLE)

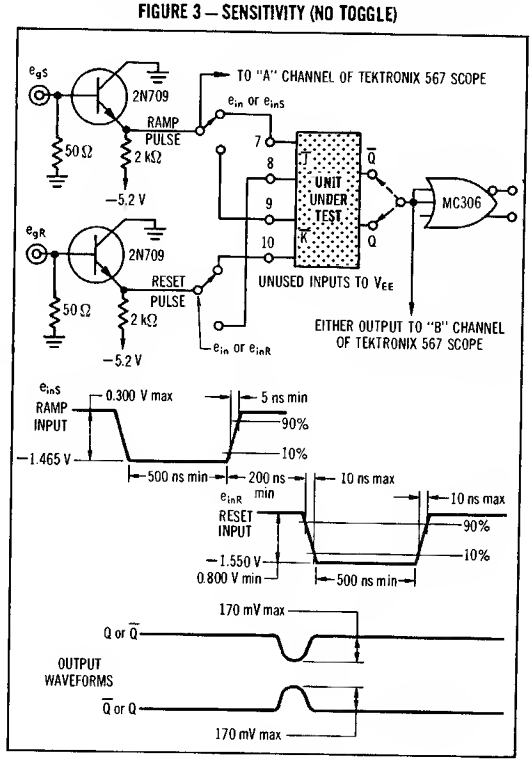
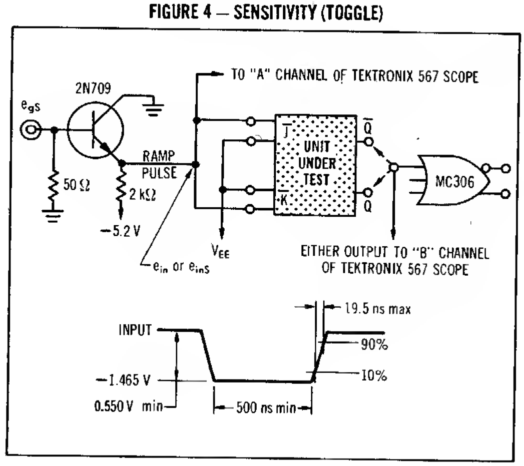


FIGURE 4 – SENSITIVITY (TOGGLE)



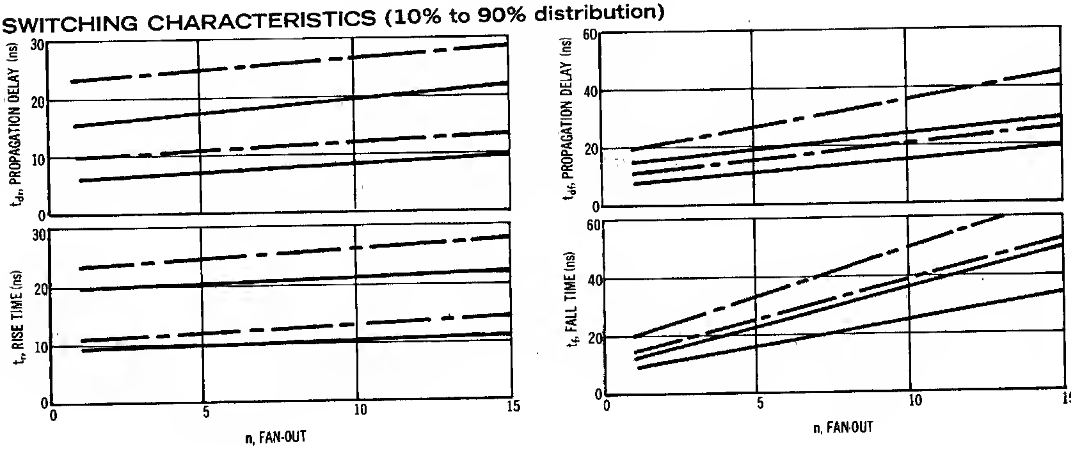
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
−55°C	—	−0.945	−1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	7,10	—	1,2,6,8,9	—	—	3	I_E (2)	—	28.5	—	28.5	—	27.5	mAdc
Input Current	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	100	—	—	µAdc
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"Q" Logical "1" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"Q" Logical "0" Output Voltage	—	—	1③	2,6,7,8,9,10	—	—	3	V_2 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"$\bar{Q}$" Logical "1" Output Voltage	—	—	1③	2,6,7,8,9,10	—	—	3	V_1 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"Q" Output Voltage Change	—	6	—	1,2,7,8,9,10	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"$\bar{Q}$" Output Voltage Change	—	1	—	2,6,7,8,9,10	—	4②	3	ΔV_1 (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.50	—	−0.65	—	−0.75	Vdc
"$\bar{Q}$" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—	−0.50	—	−0.65	—	−0.75	Vdc
"Q" or "$\bar{Q}$" Latch Voltage	—	—	—	2,7,8,9,10	1,6④	—	3	V_4 (1,6)	−1.16	−1.34	−1.09	−1.21	−0.93	−1.07	Vdc
	Pulse In	Pulse Out													
Toggle Frequency (See Figures 1 and 2)	7,10	5	—	1,2,6,9	—	—	3	f_{Tog}	—	—	30	—	—	—	MHz
Sensitivity (No Toggle)	7,10	4	—	1,2,6,8,9	—	—	3	← See Figure 3 →							
	8,9	5	—	1,2,6,7,10	—	—	3	← See Figure 3 →							
Sensitivity (Toggle)	7,10	4,5	—	1,2,6,8,9	—	—	3	← See Figure 4 →							
Switching Times									Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_{dr} (4,5)	11.0	16.0	12.0	16.0	14.0	24.0	ns
	7,10	4,5	—	1,2,6,8,9	—	—	3	t_{df} (4,5)	12.0	16.0	13.0	16.0	15.0	24.0	↓
Rise Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_r (4,5)	11.5	16.0	12.5	16.0	15.0	26.0	↓
Fall Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_f (4,5)	11.5	16.0	12.5	16.0	15.0	26.0	↓

Pins not listed are left open.
① Input voltage is adjusted to obtain $dV_{out}/dV_{in} = 0$.
② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.
③ Apply momentary $V_{I\,max}$ to set output, then V_{in} for measurement.
④ Input voltage is adjusted to obtain $dV_1/dV_{in} = \infty$.

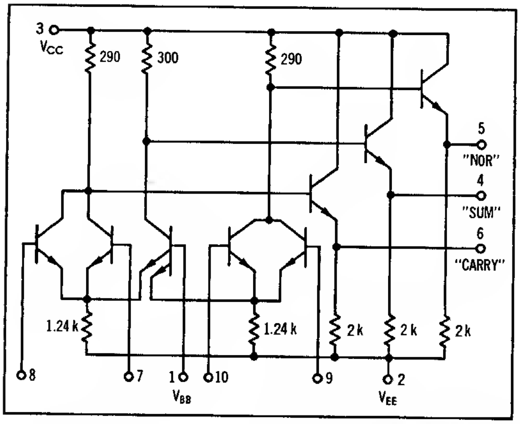
SWITCHING CHARACTERISTICS (10% to 90% distribution)



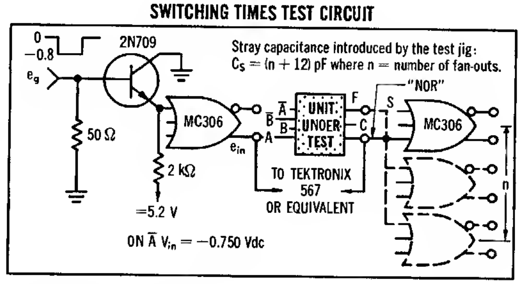
——— −55°C and +25°C
– – – +125°C

MC303

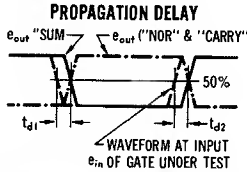
Half-adder that provides the "SUM", "CARRY", and "NOR" functions simultaneously.



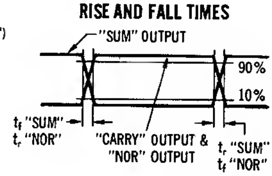
SWITCHING TIMES TEST CIRCUIT



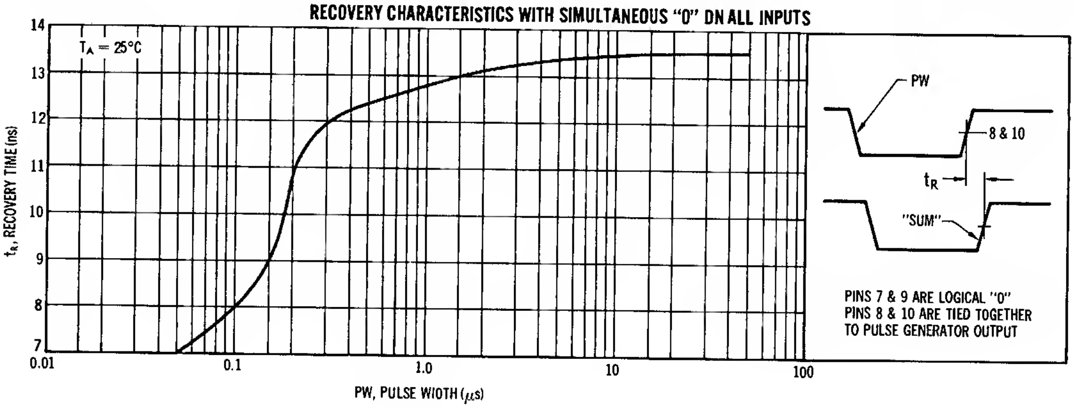
PROPAGATION DELAY



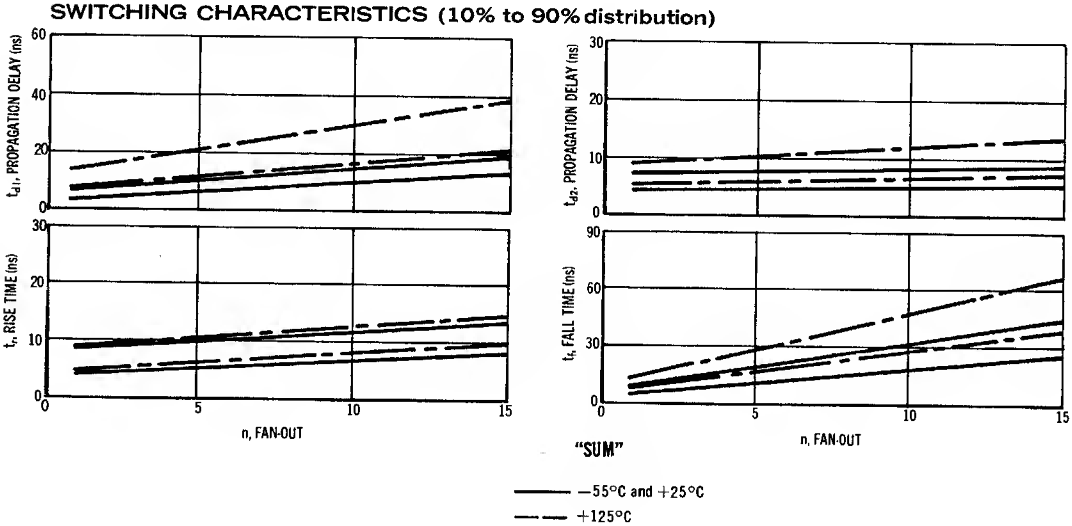
RISE AND FALL TIMES



RECOVERY CHARACTERISTICS WITH SIMULTANEOUS "0" ON ALL INPUTS



SWITCHING CHARACTERISTICS (10% to 90% distribution)



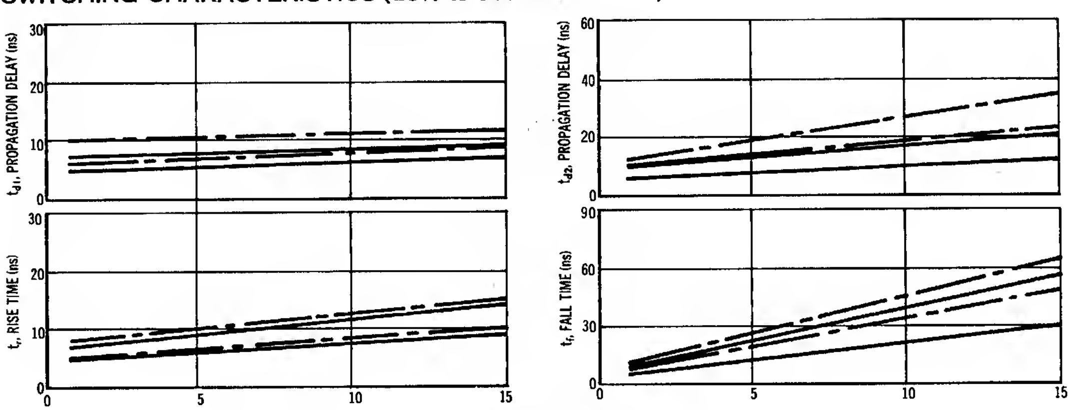
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%				
−55°C	—	−0.945	−1.450	−5.20	−1.25
+25°C	−0.690	−0.795	−1.350	−5.20	−1.15
+125°C	—	−0.655	−1.300	−5.20	−1.00

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	15.3	—	15.3	—	14.1	mAdc
Input Current	7	—	—	2,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	100	—	—	µAdc
	8	—	—	2,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,7,8,10	1	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	2,7,8,9	1	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	9	2,7,8,10	1	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	10	2,7,8,9	1	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"NOR" Logical "0" Output Voltage	—	9	—	2,7,8,10	1	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	10	—	2,7,8,9	1	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"CARRY" Logical "1" Output Voltage	—	—	7	2,8,9,10	1	—	—	3	V_1 (6)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	8	2,7,9,10	1	—	—	3	V_1 (6)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"CARRY" Logical "0" Output Voltage	—	7	—	2,8,9,10	1	—	—	3	V_4 (6)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	8	—	2,7,9,10	1	—	—	3	V_4 (6)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"SUM" Logical "1" Output Voltage	—	7,9	—	2,8,10	1	—	—	3	V_5 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	8,10	—	2,7,9	1	—	—	3	V_5 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"SUM" Logical "0" Output Voltage	—	7	10	2,8,9	1	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	8	10	2,7,9	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	8	2,7,10	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	10	7	2,8,9	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	10	—	2,7,8,9	1	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"CARRY" Output Voltage Change (No load to full load)	—	—	7	2,8,9,10	1	—	6②	3	ΔV_1 (6)	—	−0.055	—	−0.055	—	−0.060	Volts
"SUM" Output Voltage Change (No load to full load)	—	7,10	—	2,8,9	1	—	4②	3	ΔV_5 (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8,9	1	10①	—	3	V_3 (5)	—	−0.40	—	−0.55	—	−0.65	Vdc
"CARRY" Saturation Breakpoint Voltage	—	—	—	2,8,9,10	1	7①	—	3	V_3 (6)	—	−0.40	—	−0.55	—	−0.65	Vdc
Switching Times						Pulse In	Pulse Out			Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	—	—	—	2,7,8,9	1	10	5	3	t_{d1} (5)	6.0	10.0	6.0	11.0	7.5	13.0	ns
	—	—	—	2,8,9,10	1	7	6	3	t_{d1} (6)	6.0	10.0	6.0	11.0	7.5	13.0	↓
	—	7	—	2,8,9	1	10	4	3	t_{d1} (4)	8.0	12.0	8.0	12.0	10.5	17.0	↓
	—	—	—	2,7,8,9	1	10	5	3	t_{d2} (5)	7.5	10.5	7.5	11.0	10.0	15.0	↓
	—	—	—	2,8,9,10	1	7	6	3	t_{d2} (6)	7.5	10.5	7.5	11.0	10.0	15.0	↓
	—	7	—	2,8,9	1	10	4	3	t_{d2} (4)	5.5	8.0	5.5	8.5	7.5	12.0	↓
Rise Time	—	—	—	2,7,8,9	1	10	5	3	t_r (5)	6.0	11.5	6.5	12.0	7.5	14.0	↓
	—	—	—	2,8,9,10	1	7	6	3	t_r (6)	6.0	11.5	6.5	12.0	7.5	14.0	↓
	—	7	—	2,8,9	1	10	4	3	t_r (4)	6.0	10.0	6.5	11.0	10.0	16.0	↓
Fall Time	—	—	—	2,7,8,9	1	10	5	3	t_f (5)	7.5	12.0	8.0	13.5	10.5	16.5	↓
	—	—	—	2,8,9,10	1	7	6	3	t_f (6)	7.5	12.0	8.0	13.5	10.5	16.5	↓
	—	7	—	2,8,9	1	10	4	3	t_f (4)	8.0	12.5	8.5	13.5	11.0	18.0	↓

Pins not listed are left open. ① Input voltage is adjusted to obtain dV"NOR"//dV_{in} = 0 or dV "CARRY"/dV_{in} = 0.
② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



n, FAN-OUT

"NOR" and "CARRY"

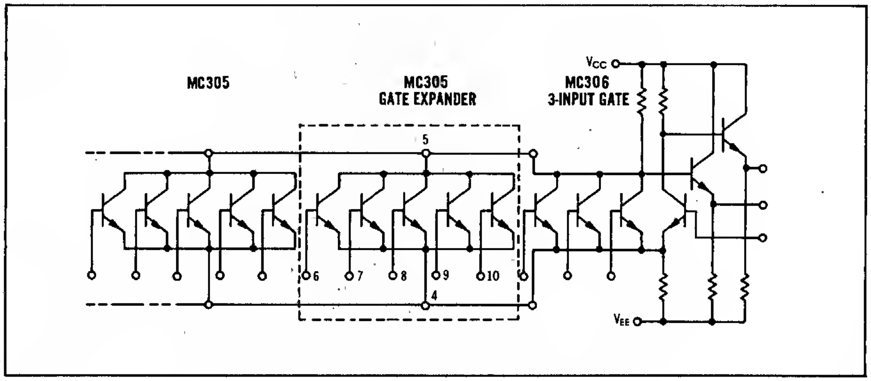
n, FAN-OUT

——— −55°C and +25°C

— — — +125°C

MC305

A 5-input expander for use with the MC302, MC306, MC307, and MC315. Each expander unit increases the fan-in of the basic gate by five.



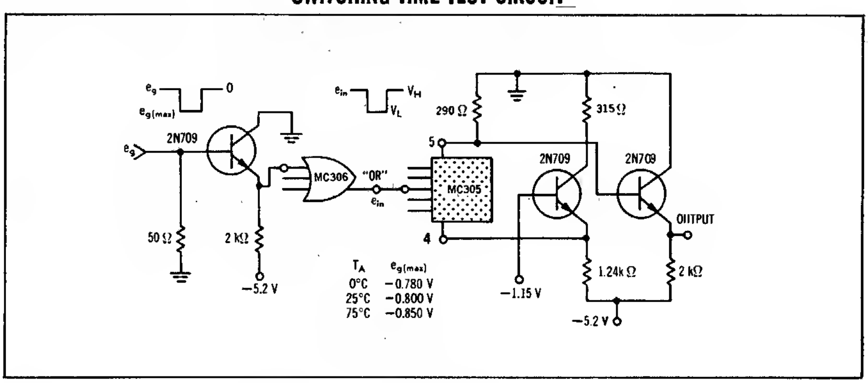
ELECTRICAL CHARACTERISTICS

	Test Conditions					
	Vdc ±1%					mAdc
@ Test Temperature −55°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33
@ Test Temperature +25°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33
@ Test Temperature +125°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33

Characteristic	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	V_{CB} Pin No	V_{BE} Pin No	I_E Pin No	Ground Pin No	Symbol Pin No in ( )	−55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Base Leakage Current	4	6	—	—	—	—	5	I_{BL} (6)	—	0.5	—	0.5	—	2.0	µAdc
	4	7	—	—	—	—	5	I_{BL} (7)	—	↓	—	↓	—	↓	↓
	4	8	—	—	—	—	5	I_{BL} (8)	—	↓	—	↓	—	↓	↓
	4	9	—	—	—	—	5	I_{BL} (9)	—	↓	—	↓	—	↓	↓
	4	10	—	—	—	—	5	I_{BL} (10)	—	↓	—	↓	—	↓	↓
Collector Leakage Current	—	—	5	—	6,7,8,9,10	—	4	I_{CEX} (5)	—	1.0	—	1.0	—	100.0	µAdc
Input Voltage	—	—	—	5	—	4	6	V_{BE} (4)	−0.810	−0.880	−0.680	−0.730	−0.490	−0.540	Vdc
	—	—	—	5	—	4	7	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	8	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	9	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	10	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
Switching Times	Pulse In / Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	8 / ①	—	—	—	—	—	—	t_{d1}	5.0	8.0	5.0	8.5	5.5	9.5	ns
	8 / ①	—	—	—	—	—	—	t_{d2}	4.0	8.0	4.0	8.0	4.5	10.0	↓
Rise Time	8 / ①	—	—	—	—	—	—	t_r	8.0	10.5	8.5	11.5	8.5	13.0	↓
Fall Time	8 / ①	—	—	—	—	—	—	t_f	3.0	8.5	3.5	8.5	4.5	9.5	↓

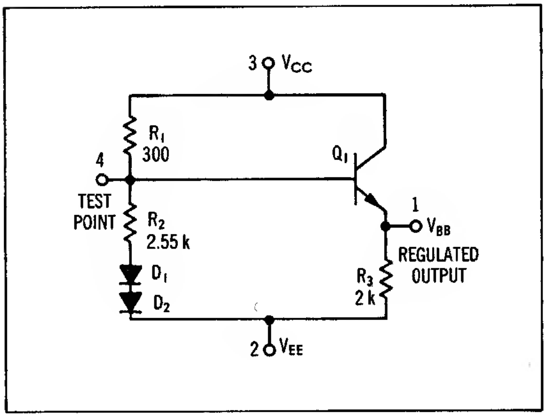
Pins not listed are left open. ① See Switching Time Test Circuit.

SWITCHING TIME TEST CIRCUIT



MC304

Bias driver that compensates for changes in circuit parameters with temperature.



ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ± 1% V_{EE}
−55°C	−5.20
+25°C	−5.20
+125°C	−5.20

Characteristic	V_{EE} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	Max	+25°C Min	Max	+125°C Min	Max	Unit
Power Supply Drain Current	2	—	3	I_E(2)	—	4.4	—	4.4	—	4.0	mAdc
Output Voltage	2	1①	3	V_{BB}	−1.19	−1.32	−1.09	−1.22	−0.95	−1.08	Vdc

Pins not listed are left open.

① Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

CIRCUIT DESCRIPTION

Circuit Operation:

The divider network R_1, R_2, D_1, D_2 compensates for temperature variations of the base-emitter voltages of Q_1, and of the driven gates, producing a bias voltage for the MECL logic circuits that maintains a constant set of dc operating conditions over the temperature range of −55 to +125°C. In addition, compensation for power supply variations is achieved, since the bias output voltage is derived from the system supply.

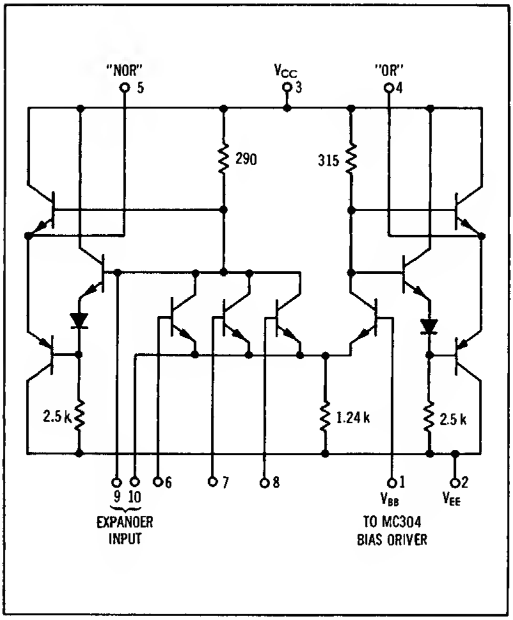
Either of the supply voltage nodes may be used as ground, however the ground potential of the bias driver must coincide with that of the logic system. Thus, if V_{CC} is grounded in the logic system, then —

$V_{CC} = 0$; $V_{EE} = -5.2$ V;

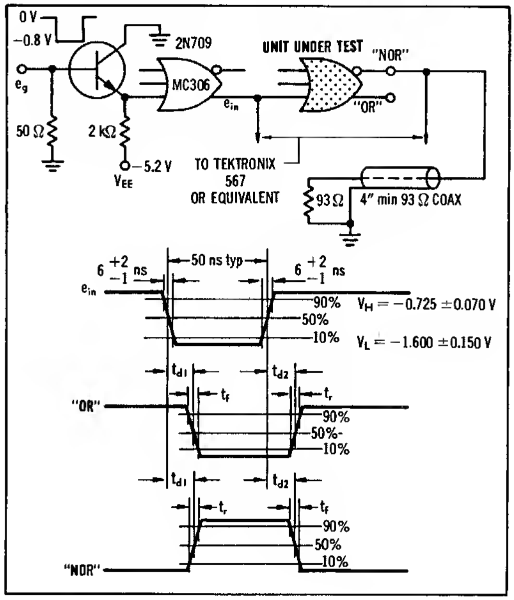
$V_{BB} = -1.15$ nominal output voltage at 25°C

MC315

Line driver for driving lines of 93 ohms or greater while providing the positive logic "NOR" function and its complement simultaneously.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



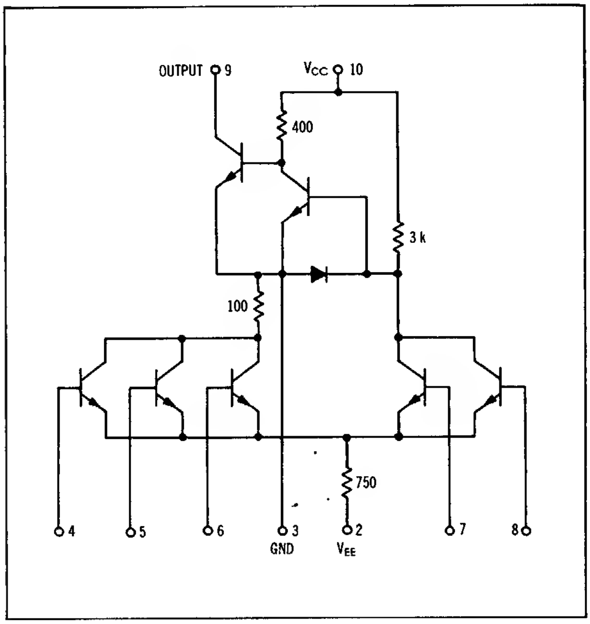
ELECTRICAL CHARACTERISTICS

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	I_L① Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Test Conditions Vdc ±1% @ Test Temperature −55°C	—	−0.945	−1.450	−5.20	−1.25										
+25°C	−0.690	−0.795	−1.350	−5.20	−1.15										
+125°C	—	−0.655	−1.300	−5.20	−1.00										
Power Supply Drain Current	—	—	—	2,6,7,8	1	4,5	3	I_E (2)	—	45	—	45	—	45	mAdc
Input Current	6	—	—	2,7,8	1	—	3	I_{in} (8)	—	—	—	100	—	—	µAdc
	7	—	—	2,8,8	1	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7	1	—	3	I_{in} (8)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8	1	4,5	3	V_1 (6)	−0.805	−0.945	−0.670	−0.795	−0.505	−0.655	Vdc
	—	—	7	2,8,8	1	4,5	3	V_1 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	4,5	3	V_1 (8)							
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8	1	4,5	3	V_4 (8)	−1.540	−1.650	−1.450	−1.750	−1.320	−1.675	Vdc
	—	7	—	2,6,8	1	4,5	3	V_4 (7)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	4,5	3	V_4 (8)							
"OR" Logical "1" Output Voltage	—	6	—	2,7,8	1	4,5	3	V_5 (8)	−0.805	−0.945	−0.870	−0.795	−0.505	−0.855	Vdc
	—	7	—	2,6,8	1	4,5	3	V_5 (7)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,8,7	1	4,5	3	V_5 (8)							
"OR" Logical "0" Output Voltage	—	—	6	2,7,8	1	4,5	3	V_2 (6)	−1.540	−1.850	−1.450	−1.750	−1.320	−1.675	Vdc
	—	—	7	2,6,8	1	4,5	3	V_2 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	4,5	3	V_2 (8)							
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	2,7,8	1	—	3	t_{d1} (5)	10.0	20.0	10.0	20.0	15.0	30.0	ns
	8	4	—	2,7,8	1	—	3	t_{d1} (4)	12.0	25.0	12.0	25.0	17.0	34.0	
	6	5	—	2,7,8	1	—	3	t_{d2} (5)	12.0	25.0	12.0	25.0	13.0	30.0	
	8	4	—	2,7,8	1	—	3	t_{d2} (4)	10.0	20.0	10.0	20.0	11.0	25.0	
Rise Time	6	5	—	2,7,8	1	—	3	t_r (5)	13.0	25.0	13.0	25.0	16.0	31.0	
	6	4	—	2,7,8	1	—	3	t_r (4)	10.0	20.0	10.0	20.0	14.5	26.0	
Fall Time	6	5	—	2,7,8	1	—	3	t_f (5)	15.0	35.0	15.0	35.0	20.0	40.0	
	6	4	—	2,7,8	1	—	3	t_f (4)	15.0	35.0	15.0	35.0	20.0	40.0	↓

Pins not listed are left open. ① Output is loaded with a 93-ohm resistor.

MC316

Lamp driver that provides "OR" or "NOR" logic depending on the bias arrangement used and is capable of driving 6V lamps.



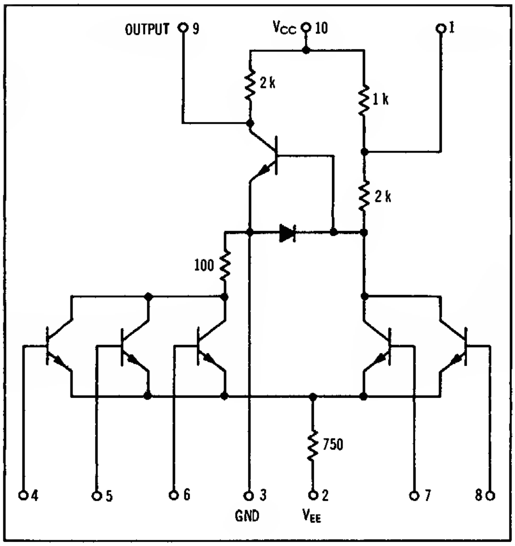
ELECTRICAL CHARACTERISTICS

	Test Conditions															
	Vdc ±1%						mAdc									
@ Test Temperature −55°C	—	−0.945	−1.450	−5.20	−1.25	+6.0	100									
@ Test Temperature +25°C	−0.670	−0.795	−1.350	−5.20	−1.15	+6.0	100									
@ Test Temperature +125°C	—	−0.655	−1.300	−5.20	−1.00	+6.0	50									
Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L② Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	4,5,8	—	2,7	8	10	—	3	I_C (10)	—	21.0	—	21.0	—	20.5	
	—	4,5,6	—	2,7	8	10	—	3	I_E (2)	—	8.0	—	8.0	—	7.7	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	µAdc
	5	—	—	2,4,8,7	8	10	—	3	I_{in} (5)	—	—	—		—	—	
	8	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—		—	—	
	7	—	—	2,4,5,8	8	10	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	2,4,5,7	8	10	—	3	I_{in} (8)	—	—	—		—	—	
Output Voltage, Low	—	—	8	2,4,5,7	8	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	0.8	
	—	—	6	2,4,5,8	7	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	0.8	
Output Voltage, High	—	4	—	2,5,6,7	8	10,9①	—	3	V_{OH} (4)	—	—	—	5.8	—	5.8	Vdc
	—	5	—	2,4,8,7	8	10,9①	—	3	V_{OH} (5)	—	—	—		—		
	—	8	—	2,4,5,7	8	10,9①	—	3	V_{OH} (8)	—	—	—		—		
	—	6	—	2,4,5,8	7	10,9①	—	3	V_{OH} (8)	—	—	—		—		

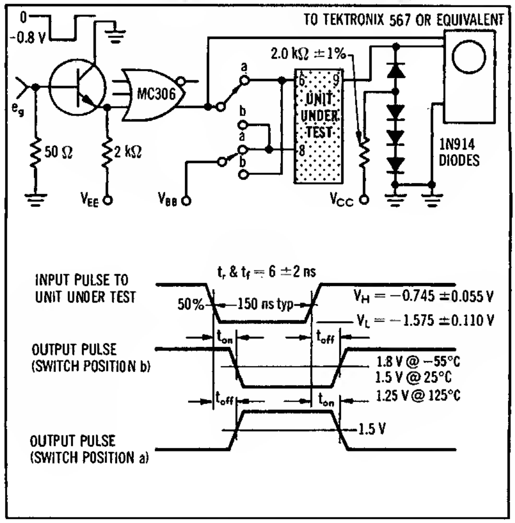
Pins not listed are left open. ① Pin 9 is connected to V_{CC} through a 10 k-ohm resistor.
② I_L specified for ambient temperature conditions. I_L = 100 mAdc at T_C = +125°C is acceptable, requiring a heat sink.

MC317

Level translator intended for converting non-saturated MECL signal levels to saturated logic levels; provides "OR" or "NOR" logic depending on the bias arrangement used.



SWITCHING TEST CIRCUIT AND WAVEFORMS

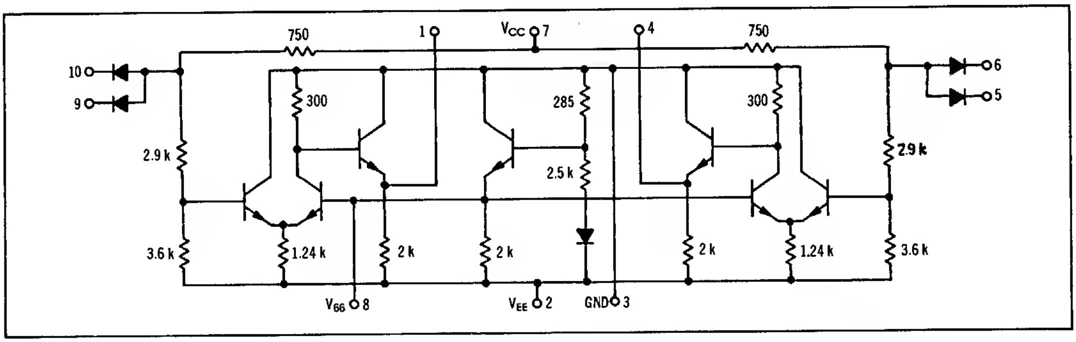


ELECTRICAL CHARACTERISTICS

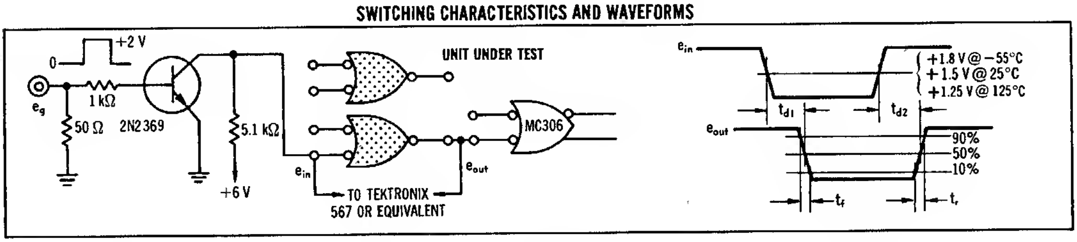
	Test Conditions															
	Vdc ±1%						mAdc									
@ Test Temperature −55°C	—	−0.945	−1.450	−5.20	−1.25	+6.0	10									
@ Test Temperature +25°C	−0.690	−0.795	−1.350	−5.20	−1.15	+6.0	10									
@ Test Temperature +125°C	—	−0.655	−1.300	−5.20	−1.00	+6.0	10									
										Test Limits						
									Symbol	−55°C		+25°C		+125°C		
Characteristic	V_H Pin No	$V_{1\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L Pin No	Ground Pin No	Pin No in ( )	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	—	6	—	2,4,5,7	8	10	—	3	I_C (10)	—	7.0	—	7.0	—	8.8	mAdc
	—	—	—	2,4,5,8,7	8	10	—	3	I_E (2)	—	7.0	—	7.0	—	6.8	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	µAdc
	5	—	—	2,4,8,7	8	10	—	3	I_{in} (5)	—	—	—	↓	—	—	↓
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	2,4,5,8	6	10	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,4,5,7	8	10	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
Output Voltage, High	—	—	—	2,4,5,6,7	8	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
	—	—	—	2,4,5,8,8	7	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
Output Voltage, Low	—	4	—	2,5,6,7	8	10	9	3	V_{OL} (9)	—	0.45	—	0.45	—	0.50	Vdc
	—	5	—	2,4,8,7	8	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
	—	6	—	2,4,5,7	8	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
	—	6	—	2,4,5,8	7	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Turn-On Time	8	9	—	2,4,5,7	8	10	—	3	t_{on}	27.5	40.0	27.5	35.0	29.5	35.0	ns
	8	9	—	2,4,5,7	6	10	—	3	t_{on}	27.5	40.0	27.5	35.0	29.5	35.0	↓
Turn-Off Time	6	9	—	2,4,5,7	8	10	—	3	t_{off}	25.0	40.0	26.0	35.0	27.0	40.0	↓
	8	9	—	2,4,5,7	6	10	—	3	t_{off}	25.0	40.0	26.0	35.0	27.0	40.0	↓

MC318

Level translator intended for converting saturated logic levels to non-saturated MECL signal levels.



SWITCHING CHARACTERISTICS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
−55°C	+0.45	+5.0	−5.20	+6.0
+25°C	+0.45	+5.0	−5.20	+6.0
+125°C	+0.45	+5.0	−5.20	+6.0

Characteristic	V Pin No	V Pin No	V_{EE} Pin No	V_{CC} Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	— —	— —	2 2	7 7	3 3	I_C (7) I_E (2)	— —	4.0 24.0	— —	4.0 24.0	— —	3.9 23.3	mAdc mAdc
Input Load Current	— — — —	— — — —	2 2 2 2	7 7 7 7	3,5 3,6 3,9 3,10	I_L (5) I_L (6) I_L (9) I_L (10)	— — — —	— — — —	— — — —	8.0 ↓	— — — —	— — — —	mAdc ↓
Input Reverse Current	— — — —	— — — —	2 2 2 2	5,7 6,7 7,9 7,10	3,6 3,5 3,10 3,9	I_R (5) I_R (6) I_R (9) I_R (10)	— — — —	— — — —	— — — —	0.5 ↓	— — — —	2.0 ↓	µAdc ↓
"OR" Logical "1" Output Voltage	— — — —	5 6 9 10	2 2 2 2	7 7 7 7	3 3 3 3	V_S (4) V_S (4) V_S (1) V_S (1)	−0.825 ↓	−0.945 ↓	−0.690 ↓	−0.795 ↓	−0.525 ↓	−0.655 ↓	Vdc ↓
"OR" Logical "0" Output Voltage	5 6 9 10	— — — —	2 2 2 2	7 7 7 7	3 3 3 3	V_2 (4) V_2 (4) V_2 (1) V_2 (1)	−1.560 ↓	−1.850 ↓	−1.465 ↓	−1.750 ↓	−1.340 ↓	−1.675 ↓	Vdc ↓
Bias Voltage Output Current	—	—	2	7	3	V_{BB} (8)	−1.19 ↓	−1.32 ↓	−1.09 ↓	−1.22 ↓	−0.95 ↓	−1.08 ↓	Vdc ↓
Switching Times	Pulse In	Pulse Out					Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	5 9	4 1	2 2	7 7	3 3	t_{d1} (4) t_{d1} (1)	16.5 16.5	27.0 27.0	15.0 15.0	23.0 23.0	19.0 19.0	28.0 28.0	ns
	5 9	4 1	2 2	7 7	3 3	t_{d2} (4) t_{d2} (1)	13.0 13.0	20.0 20.0	15.5 15.5	23.0 23.0	20.0 20.0	31.0 31.0	↓
Rise Time	5 9	4 1	2 2	7 7	3 3	t_r (4) t_r (1)	8.0 6.0	15.0 15.0	7.0 7.0	13.0 13.0	9.5 9.5	16.0 16.0	↓
Fall Time	5 9	4 1	2 2	7 7	3 3	t_f (4) t_f (1)	6.0 6.0	14.0 14.0	7.5 7.5	13.0 13.0	10.0 10.0	17.0 17.0	↓

Pins not listed are left open.

MECL

INTEGRATED CIRCUITS

INDEX

MC350 Series

NUMERICAL INDEX
(Functions and Characteristics)

$V_{CC} = 0$, $V_{EE} = -5.2$ V, $T_A = 25°C$

Function	Type ①	DC Output Loading Factor Each Output	Propagation Delay tpd ns typ	Total Power Dissipation mW typ/pkg	Case	Page No.
5-Input OR/NOR Gate	MC351	25	7.5	37	71, 72	2-44
R-S Flip-Flop	MC352A		11	42		2-52
Half-Adder	MC353		7.5	63		2-58
Bias Driver	MC354		–	18		2-61
5-Input Gate Expander	MC355	–	4.5	–		2-60
3-Input OR/NOR Gate	MC356	25	7.5	37		2-41
3-Input OR/NOR Gate	MC357		7.5	15		2-41
AC-Coupled J-K Flip-Flop	MC358A		8.5	87		2-54
Dual 2-Input NOR Gate	MC359		7.0	54		2-46
Dual 2-Input NOR Gate	MC360		7.0	54		2-46
Dual 2-Input NOR Gate	MC361		7.0	41		2-46
Dual 3-Input NOR Gate (With Internal Bias)	MC362A		7.5	70		2-48
Quad 2-Input NOR Gate	MC363F		7.0	125	83	2-50
AC-Coupled J-K Flip-Flop	MC364		12	118	71, 72	2-56
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Lamp Driver	MC366	–	–	135		2-67
Level Translator – MECL to Saturated Logic	MC367	7 (DTL)	27.5	63		2-68
Level Translator – Saturated Logic to MECL	MC368	25 (MECL)	17	105	71, 72	2-69
Dual 4-Input Clock Driver/High-Speed Gate	MC369F	100	3.0	250	83	2-65
Dual 2-Input Clock Driver/High-Speed Gate	MC369G	100	3.0	250	71	2-63

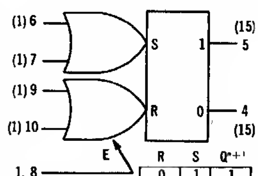
① G suffix denotes Metal Can, F suffix denotes Flat Package. (i.e., MC351G = Metal Can, MC351F = Flat Package.)
② With 50-ohm load (each side)

POSITIVE LOGIC: V_H is a logical "1", V_L is a logical "0"
NEGATIVE LOGIC: V_H is a logical "0", V_L is a logical "1"

The logic diagrams shown describe the circuits of the MC350 line and permit quick selection of those circuits required for the implementation of this particular logic system. Pertinent information such as logic equations, typical time delay, typical power dissipation, and truth tables is provided to show line compatibility. Package pin numbers and fan-in and fan-out for each device are specified on each logic diagram. The numbers at the ends of the terminals are package pin numbers. The numbers in parentheses indicate ac loading factors at each terminal.

MECL circuits require a bias voltage which, for best results, should be obtained from a regulated, temperature-compensated, bias supply. A bias driver, type MC354, is included in the MECL line to provide this function when the bias driver is not contained in the logic element. Specifications for the bias driver are given on page 2—61

MC352A — R-S FLIP-FLOP



R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

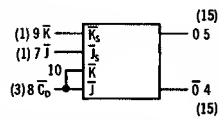
t_{dr} = 10.5 ns
P_D = 42 mW

DC Set-Reset flip-flop with expandable input and buffered outputs. This flip-flop is available without buffered outputs as MC352.

MC358A — AC-COUPLED J-K FLIP-FLOP

CLOCKED J-K OPERATION

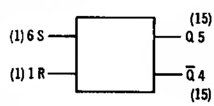
$\bar{J}_s$	$\bar{K}_s$	$\bar{C}_D$	Q^{n+1}
φ	φ	0	Q^n
0	0	1	$\bar{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n



The $\bar{J}_s$ and $\bar{K}_s$ inputs refer to logic levels while the $\bar{C}_D$ input refers to dynamic logic swings. The $\bar{J}_s$ and $\bar{K}_s$ inputs would be changed to a logical "1" only while the $\bar{C}_D$ input is in a logic "1" state. ($\bar{C}_D$ maximum "1" level = V_{CC} − 0.6 volts)

R-S OPERATION

R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



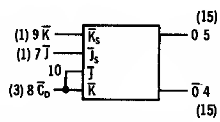
t_{dr} = 7.5 ns
P_D = 87 mW

AC-Coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.

MC364 — AC-COUPLED J-K FLIP-FLOP

CLOCKED J-K OPERATION

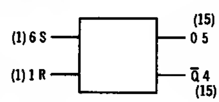
$\bar{J}$	$\bar{K}$	$\bar{C}$	Q^{n+1}
φ	φ	0	Q^n
0	0	1	$\bar{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n



The $\bar{J}$ and $\bar{K}$ inputs refer to logic levels while the $\bar{C}_D$ input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to a logical "1" only while the $\bar{C}_D$ input is in a logic "1" state. ($\bar{C}_D$ maximum "1" level = V_{CC} − 0.6 volts)

R-S OPERATION

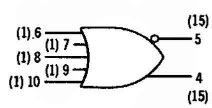
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



t_{dr} = 12 ns
P_D = 118 mW

High-speed ac-coupled J-K flip-flop with dc Set and Reset inputs for counter and shift register applications up to 30 MHz operation.

MC351 — 5-INPUT GATE

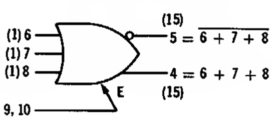


$5 = \overline{6 + 7 + 8 + 9 + 10}$
$4 = 6 + 7 + 8 + 9 + 10$

t_{dl} = 7.5 ns
P_D = 37 mW

Provides the positive logic "NOR" function and its complement simultaneously.

MC356 — 3-INPUT GATE

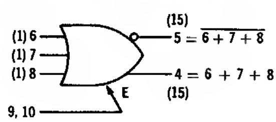


$5 = \overline{6 + 7 + 8}$
$4 = 6 + 7 + 8$

t_{dl} = 7.0 ns
P_D = 37 mW

Provides the positive logic "NOR" function and its complement simultaneously.

MC357 — 3-INPUT GATE

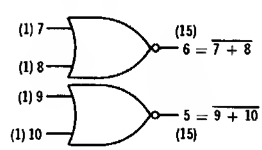


$5 = \overline{6 + 7 + 8}$
$4 = 6 + 7 + 8$

t_{dl} = 7.0 ns *No pull-down resistors
P_D = 15 mW

Provides the positive logic "NOR" function and its complement simultaneously. Same as MC356, with pull-down resistors omitted, permitting a reduction of power dissipation (see schematic diagram on page 2-41).

MC359 — DUAL 2-INPUT GATE



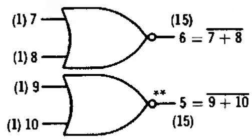
$6 = \overline{7 + 8}$
$5 = \overline{9 + 10}$

t_{dl} = 6.5 ns
P_D = 27 mW/gate

Provides the positive logic "NOR" function.

LOGIC DESCRIPTION (continued)

MC360 — DUAL 2-INPUT GATE

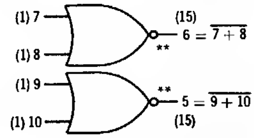


**Optional pull-down resistor. If resistor is desired, connect pin 4 to pin 5.

$t_{d1} = 6.5$ ns $P_D = 27$ mW/gate

Provides the positive logic "NOR" function. Same as MC359 with one output pull-down resistor optional (see schematic diagram on page 2-46).

MC361 — DUAL 2-INPUT GATE

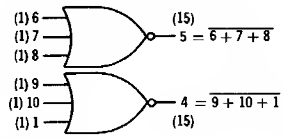


**Optional pull-down resistor. If resistor is desired, connect pin 4 to pin 5 or pin 6.

$t_{d1} = 6.5$ ns $P_D = 21$ mW/gate

Provides the positive logic "NOR" function. Same as MC359 with one output pull-down resistor omitted and the second optional (see schematic diagram on page 2-46).

MC362A — DUAL 3-INPUT GATE

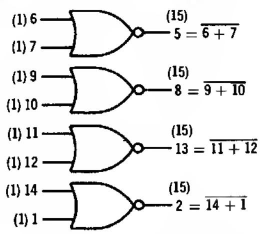


$t_{d1} = 7.5$ ns

$P_D = 35$ mW/gate

Provides the positive logic "NOR" function, and features an internal bias driver. This gate without the bias driver is available as the MC362.

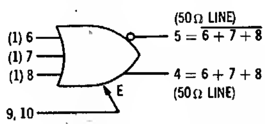
MC363F — QUAD 2-INPUT GATE



$t_{d1} = 6.5$ ns $P_D = 31$ mW/gate

Provides the positive logic "NOR" function, and features an internal bias driver.

MC365 — LINE DRIVER

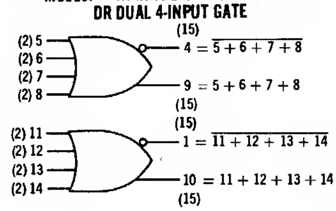


$t_{d1} = 14$ ns

$P_D = 270$ mW (with 50 Ω load)

Drives lines of 50 ohms or greater while providing the positive logic "NOR" function and its complement simultaneously.

MC369F — HIGH-SPEED CLOCK DRIVER OR DUAL 4-INPUT GATE

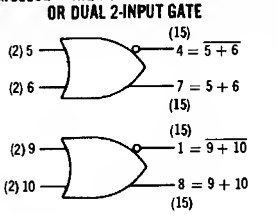


$t_{d1} = 3$ ns

$P_D = 125$ mW/gate

Provides the positive logic "NOR" function and its complement simultaneously.

MC369G — HIGH-SPEED CLOCK DRIVER OR DUAL 2-INPUT GATE

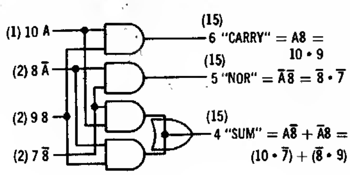


$t_{d1} = 3$ns

$P_D = 125$ mW/gate

Provides the positive logic "NOR" function and its complement simultaneously.

MC353 — HALF-ADDER

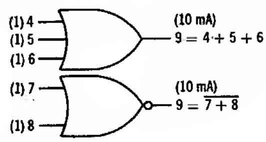


$t_{d1} = 7$ ns

$P_D = 63$ mW

Provides the "SUM", "CARRY", and "NOR" functions simultaneously. If complement inputs are not used, an undefined state can occur.

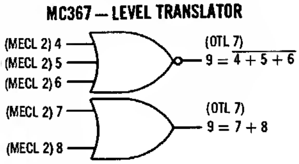
MC366 — LAMP DRIVER



$P_D = 135$ mW

Capable of driving 6-volt lamps. Positive "NOR" function is obtained by applying V_{BB} to pin 4, 5, or 6, with pins 7 and 8 used as inputs. Positive "OR" is obtained by applying V_{BB} to pin 7 or 8, with pins 4, 5, and 6 used as inputs.

MC367 — LEVEL TRANSLATOR

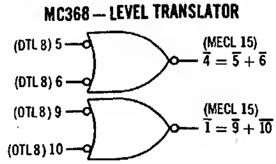


$t_{dr} = 30$ ns

$P_D = 63$ mW

Intended for converting non-saturated MECL signal levels to saturated logic levels. Positive "NOR" function is obtained by applying V_{BB} to pin 7 or 8, with pins 4, 5, and 6 used as inputs. Positive "OR" is obtained by applying V_{BB} to pin 4, 5, or 6, with pins 7 and 8 used as inputs.

MC368 — LEVEL TRANSLATOR

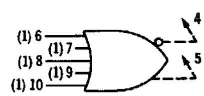


$t_{d1} = 17$ ns

$P_D = 105$ mW

Intended for converting saturated logic levels to non-saturated MECL signal levels. By applying DTL input logic levels as defined by logical "0" at 0.4 V and logical "1" at 5.0 V, corresponding MECL outputs are obtained as defined by logical "0" at −1.55 V and logical "1" at −0.75 V.

MC355 — 5-INPUT EXPANDER



$t_{d1} = 5$ ns

For use with the MC352A, MC356, MC357, and MC365. Each expander unit increases the fan-in of the basic gate by five. For highest performance, a maximum of three expander units per gate is recommended.

CIRCUIT DESCRIPTION

The MECL line of monolithic integrated logic circuits was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic, and permits extremely high-speed operation.

The typical MECL circuit comprises a differential-amplifier input, with emitter-follower output to restore dc levels. High fan-out operation is possible because of the high input impedance of the differential amplifier and the low output impedance of the emitter followers. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the function and its complement.

POWER-SUPPLY CONNECTIONS

Any one of the power supply nodes, V_{BB}, V_{CC}, or V_{EE} may be used as ground; however, the manufacturer has found it most convenient to ground the V_{CC} node. In such a case: $V_{CC} = 0$, $V_{BB} = -1.15$ V, $V_{EE} = -5.2$ V, as shown in the schematic diagram above.

SYSTEM LOGIC SPECIFICATIONS

The output logic swing of 0.8 V then varies from a low state of $V_L = -1.55$ V to a high state of $V_H = -0.75$ V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's". Then

$$\left.\begin{aligned}``0" &= -1.55\ \text{V}\\ ``1" &= -0.75\ \text{V}\end{aligned}\right\}\ \text{typical}$$

Dynamic logic refers to a change of logic states. Dynamic "0" is a negative going voltage excursion and a dynamic "1" is a positive going voltage excursion.

CIRCUIT OPERATION

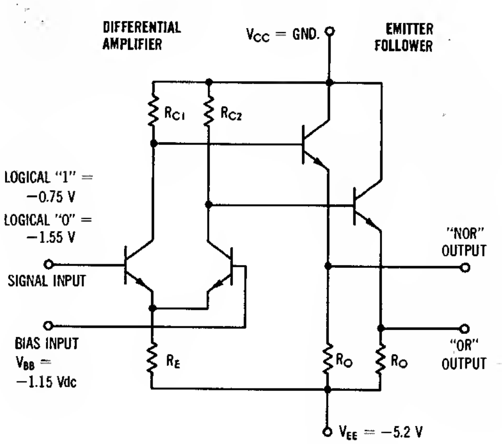
A fixed bias of -1.15 volts is applied to the "bias input" of the differential amplifier and the logic signals are applied to the "signal input". If a logical "0" is applied, the current through R_E is supplied by the fixed-biased transistor. A drop of 800 mV occurs across R_{C2}. The OR output then is -1.55 V, or one V_{BE}-drop below 800 mV. Since no current flows in the "signal input" transistor, the NOR output is a V_{BE}-drop below ground, or -0.75 volts. When a logical "1" level is applied to the "signal input", the current through R_{C2} is switched to the "signal input" transistor and a drop of 800 mV occurs across R_{C1}. The OR output then goes to -0.75 volts and the NOR output goes to -1.55 volts.

Note: Any unused input should be connected to V_{EE}.

BIAS VOLTAGE SOURCE

The bias voltage applied to the bias input is obtained from a regulated, temperature-compensated bias driver, type MC354. The temperature characteristics of the bias driver compensate for any variations in circuit operating point over the temperature range or supply voltage changes, to insure that the threshold point is always in the center of the transition region. The bias driver can be used to drive up to 25 logic elements and should be employed for all elements except those with built-in bias networks.

BASIC MECL GATE CIRCUIT



FOR LOGICAL "1" INPUT, "NOR" OUTPUT = −1.55 V
"OR" OUTPUT = −0.75 V
FOR LOGICAL "0" INPUT, "NOR" OUTPUT = −0.75 V
"OR" OUTPUT = −1.55 V

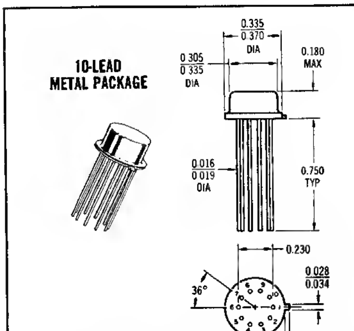
DEFINITIONS

- e_{in} — AC signal applied to the input
- e_{out} — AC signal at the output
- I_C — Amount of current drawn from the positive power supply by the test unit
- I_{CEX} — Total collector leakage current exhibited by the gate expander when all inputs are at the negative supply potential
- I_E — Amount of current drawn from the test unit by the negative power supply
- I_{in} — Current drawn by the input of the test unit when a logical "1" (V_H) is applied to the input
- I_L — Current drawn from a node when that node is at ground potential
- t_{d1} — Time required for the output pulse to reach the 50% point of its leading edge when referenced to the 50% point of the input pulse leading edge
- t_{d2} — Time required for the output pulse to reach the 50% point of its trailing edge when referenced to the 50% point of the input pulse trailing edge
- t_{df} — Time required for a flip-flop output to reach the 50% point of its negative going edge when referenced to the 50% point of the input pulse leading edge
- t_{dr} — Time required for a flip-flop output to reach the 50% point of its positive going edge when referenced to the 50% point of the input pulse leading edge
- t_f — Time required for the output pulse to go more negative from its 90% point to its 10% point
- t_r — Time required for the output pulse to go more positive from its 10% point to its 90% point
- V_1 — "NOR" output voltage – logical "1" level output voltage when a logical "0" level (V_L) is applied to the input
- V_2 — "OR" output voltage – logical "0" level output voltage when a logical "0" level (V_L) is applied to the input
- V_3 — Saturation breakpoint voltage which corresponds to the "NOR" output characteristic where the rate of change in the output voltage to the rate of change in input voltage is zero
- V_4 — "NOR" output voltage – logical "0" level output voltage when a logical "1" level ($V_{1\ max}$) level is applied to the input
- V_5 — "OR" output voltage – logical "1" level output voltage when a logical "1" ($V_{1\ max}$) level is applied to the input
- V_6 — Output latch voltage – input voltage to a flip-flop which causes the output voltage to change from a logical "1" level to a logical "0" level and corresponds to the point where the rate of change in the output voltage to the rate of the input voltage approaches infinity
- V_H — Logical "1" input voltage
- V_L — Logical "0" input voltage
- V_{OH} — High-level output voltage when the saturated logic circuit output is in an "off" condition
- V_{OL} — Low-level output voltage when the saturated logic output circuit is in an "on" condition
- ΔV_1, ΔV_5 — Change in the "1" level output voltage as the load is varied from no load to full load

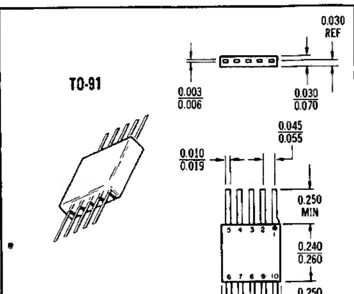
PACKAGES

All MECL integrated circuits are available in both the TO-91, 10-lead flat package and the 10-lead metal package. To order the flat package, add suffix "F" to basic type number; to order metal package, add suffix "G".

Exceptions: Types MC363F and MC369F are available only in the TO-86, 14-lead flat package; type MC369G is available only in the metal package.

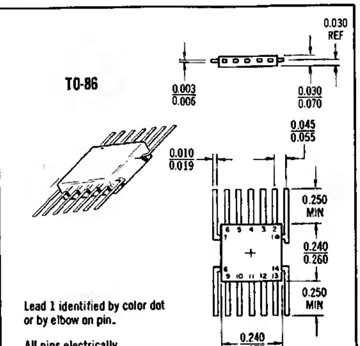


MC355 – Pin 5 connected to case
All other types – Pin 2 connected to case



Lead 1 identified by color dot or by shoulder on pin.

All pins electrically isolated from package.



Lead 1 identified by color dot or by elbow on pin.

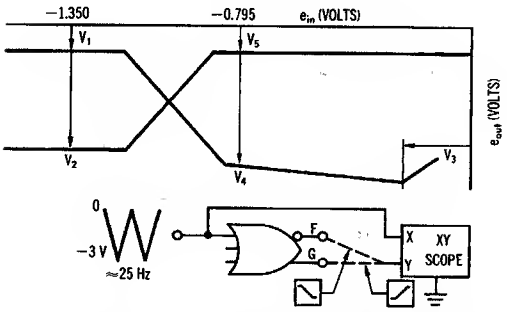
All pins electrically isolated from package.

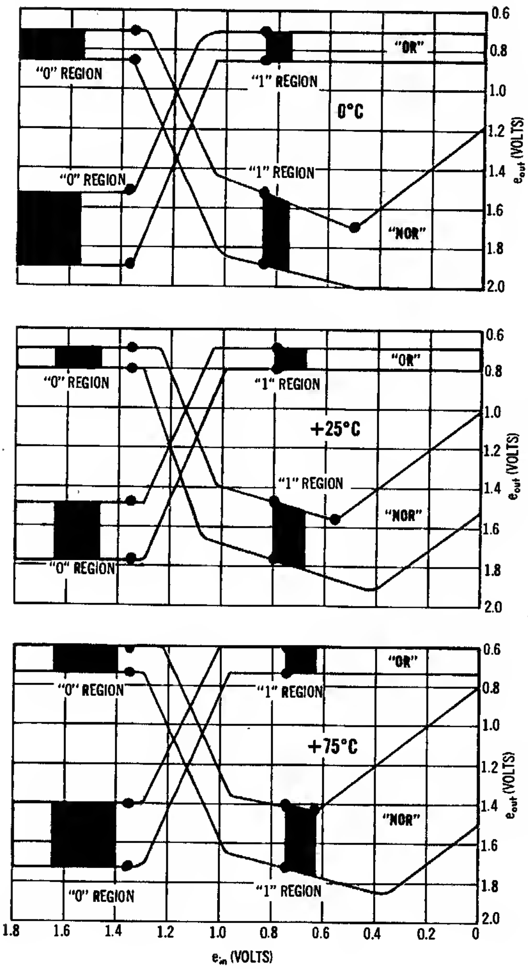
GENERAL INFORMATION (continued)

WORST-CASE TRANSFER CHARACTERISTICS

The following graphs show minimum and maximum limits of major parameters associated with the transfer characteristics of the MECL line. Min-Max limits, given at three different temperatures can be interpreted for design purposes as 10% to 90% spreads at all points on the curve except for guaranteed points in the Electrical Characteristics tables.

DEFINITIONS





MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage ($V_{CC} = 0$)	V_{EE}	−10	Vdc
Base Input Voltage ($V_{CC} = 0$)	V_{in}	0 Vdc to V_{EE}	Vdc
Output Source Current	I_O	20	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	0 to +75	°C
AC Fan-In (Expandable Gates)	m	18	—
AC Fan-Out* (Gates and Flip-Flops)	n	15	—

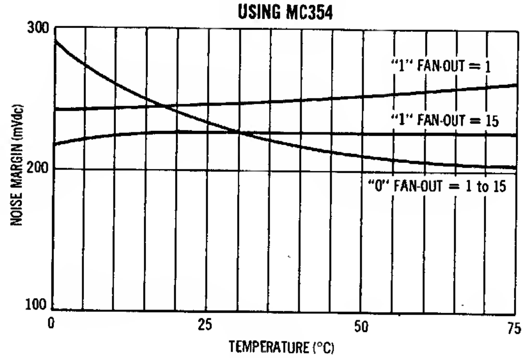
*Although a minimum dc fan-out of 25 is guaranteed in each electrical specification, it is recommended that the maximum ac fan-out of 15 be used for high-speed operation.

NOISE MARGINS (90 PERCENTILE)

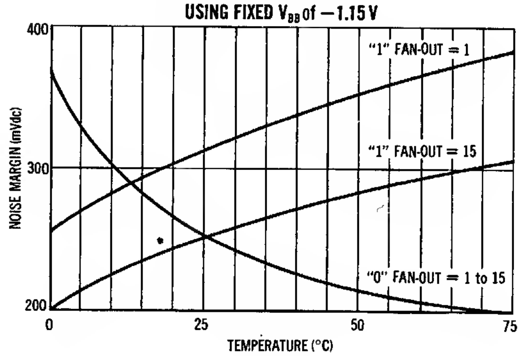
The following graphs show worst-case Noise Margins as a function of temperature and fan-out. Top graph illustrates the advantage gained through use of MC354 bias driver, as compared with non-compensated fixed bias source, bottom.

Note: Any unused input should be connected to V_{EE}.

USING MC354

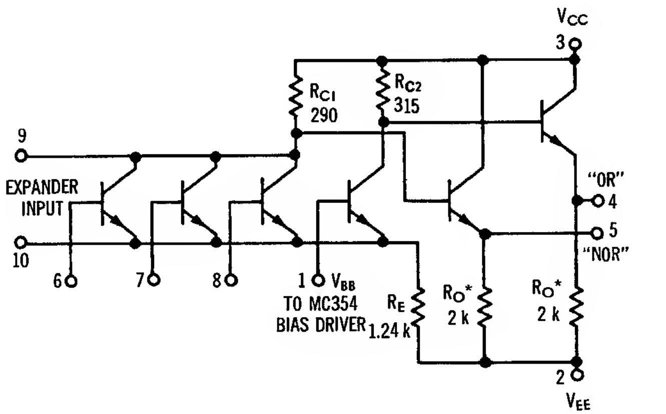


USING FIXED V_{BB} of −1.15 V



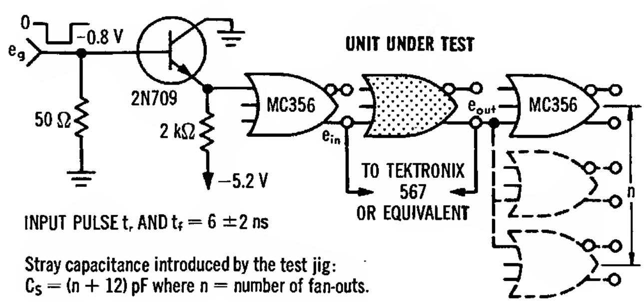
MC356 • MC357

Expandable 3-input gates that provide the positive logic "NOR" function and its complement simultaneously. MC357 omits output pull-down resistors, permitting reduction of power dissipation.



*Resistors R_O are omitted in MC357 circuits to permit reduction of Power Dissipation in systems where logic operations are performed at circuit outputs.

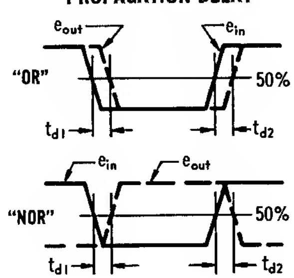
SWITCHING TIME TEST CIRCUIT



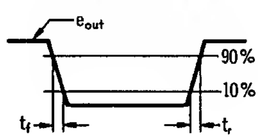
INPUT PULSE t_r AND t_f = 6 ±2 ns

Stray capacitance introduced by the test jig:
C_S = (n + 12) pF where n = number of fan-outs.

PROPAGATION DELAY

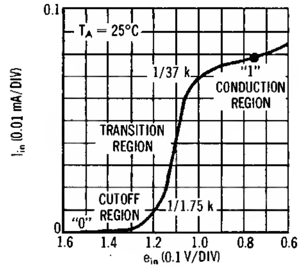


RISE AND FALL TIME

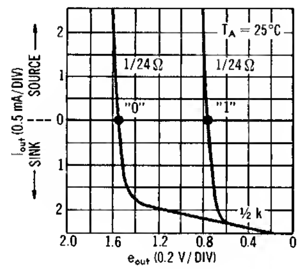


Fan-in obtained with MC355 input expanders; all but driven input connected to −5.2 V.

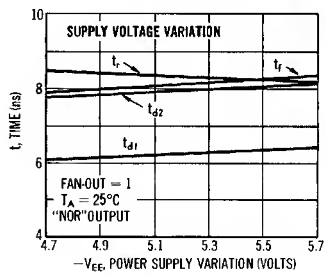
TYPICAL INPUT CHARACTERISTICS

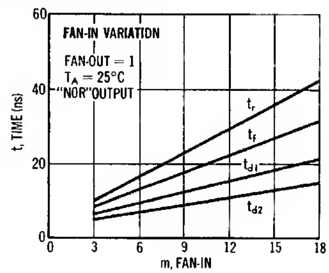


TYPICAL OUTPUT CHARACTERISTICS

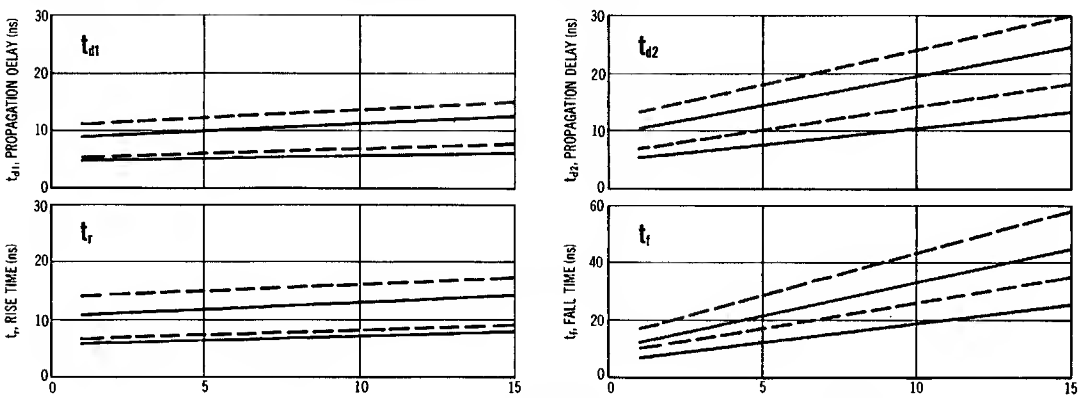


TYPICAL SWITCHING TIME VARIATIONS MC356





SWITCHING CHARACTERISTICS (10% to 90% distribution)



"NOR" OUTPUT

——— 0°C and +25°C

– – – +75°C

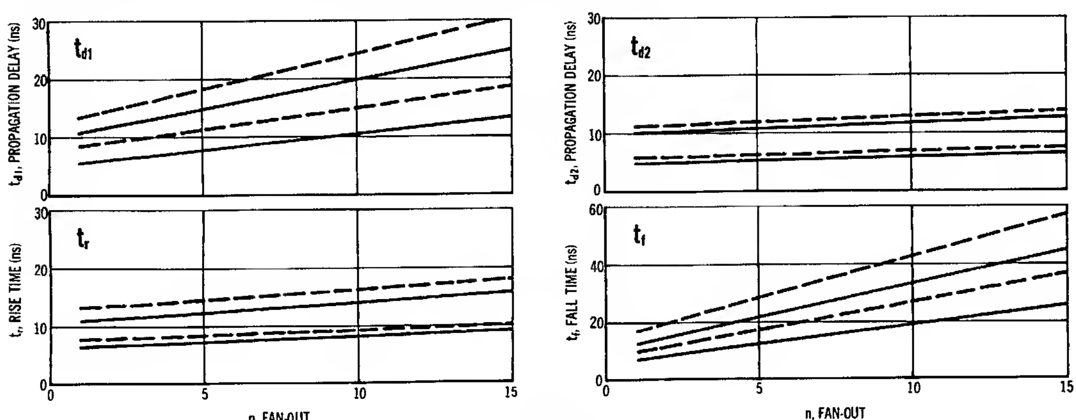
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%				
	V_H	$V_{I\,max}$	V_L	V_{EE}	V_{EB}
0°C	—	−0.850	−1.350	−5.20	−1.18
+25°C	−0.670	−0.795	−1.350	−5.20	−1.15
+75°C	—	−0.725	−1.350	−5.20	−1.08

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{EB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current MC358	—	—	—	2,6,7,8	1	—	—	3	I_E (2)	—	9.25	—	8.85	—	8.15	mAdc
MC357	—	—	—	2,6,7,8	1	—	—	3	I_E (2)	—	3.8	—	3.6	—	3.3	mAdc
Input Current	6	—	—	2,7,8	1	—	—	3	I_{in} (6)	—	—	—	100	—	—	µAdc
	7	—	—	2,6,8	1	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7	1	—	—	3	I_{in} (8)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8	1	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	2,6,8	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	—	—	3	V_1 (5)							
"NOR" Logical "0" Output Voltage	—	8	—	2,7,8	1	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	7	—	2,6,8	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	—	—	3	V_4 (5)							
"OR" Logical "1" Output Voltage	—	6	—	2,7,8	1	—	—	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	7	—	2,6,8	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	—	—	3	V_5 (4)							
"OR" Logical "0" Output Voltage	—	—	6	2,7,8	1	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	—	7	2,6,8	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	—	—	3	V_2 (4)							
"NOR" Output Voltage Change (No load to full load)	—	—	6	2,7,8	1	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.065	Volts
"OR" Output Voltage Change (No load to full load)	—	6	—	2,7,8	1	—	4②	3	ΔV_5 (4)	—	−0.055	—	−0.055	—	−0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8	1	6①	—	3	V_3 (5)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	2,6,8	1	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7	1	8①	—	3	V_3 (5)	—		—		—		
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	4	—	2,7,8	1	—	—	3	t_{d1} (4)	8.5	11.5	8.5	11.5	10.0	15.0	ns
	6	5	—	2,7,8	1	—	—	3	t_{d1} (5)	6.5	10.5	6.5	10.5	7.5	11.5	↓
	6	4	—	2,7,8	1	—	—	3	t_{d2} (4)	6.0	11.0	6.0	11.0	7.5	12.0	
	6	5	—	2,7,8	1	—	—	3	t_{d2} (5)	8.5	11.5	8.5	11.5	10.0	15.0	
Rise Time	8	4	—	2,7,8	1	—	—	3	t_r (4)	7.0	11.5	7.0	11.5	9.0	13.0	
	6	5	—	2,7,8	1	—	—	3	t_r (5)	9.0	12.5	9.5	12.5	11.5	15.5	
Fall Time	6	4	—	2,7,8	1	—	—	3	t_f (4)	9.0	14.0	9.5	14.0	12.0	17.0	
	6	5	—	2,7,8	1	—	—	3	t_f (5)	8.5	14.0	9.0	14.0	11.5	17.0	

Pins not listed are left open ① Input voltage is adjusted to obtain dV "NOR/dV_{in} = 0. ② Current test conditions: no load = 0; full load = −2.5mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

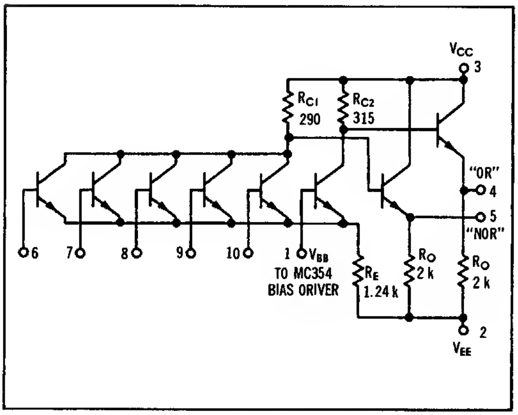


"OR" OUTPUT

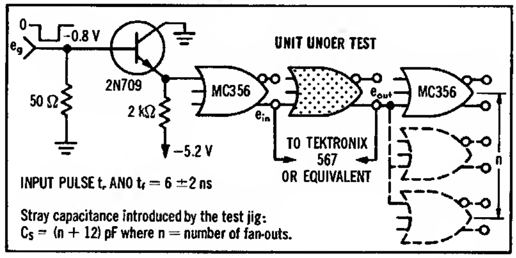
——— 0°C and +25°C
– – – – +75°C

MC351

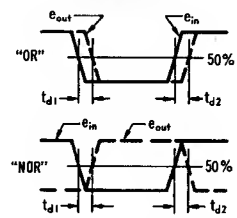
A 5-input gate that provides the positive logic "OR" function and its complement simultaneously.



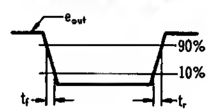
SWITCHING TIME TEST CIRCUIT



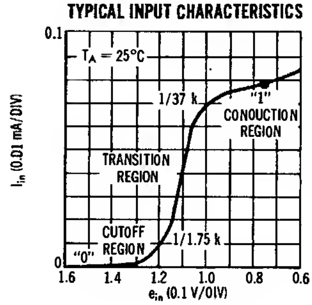
PROPAGATION DELAY



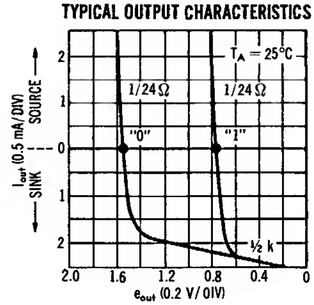
RISE AND FALL TIME



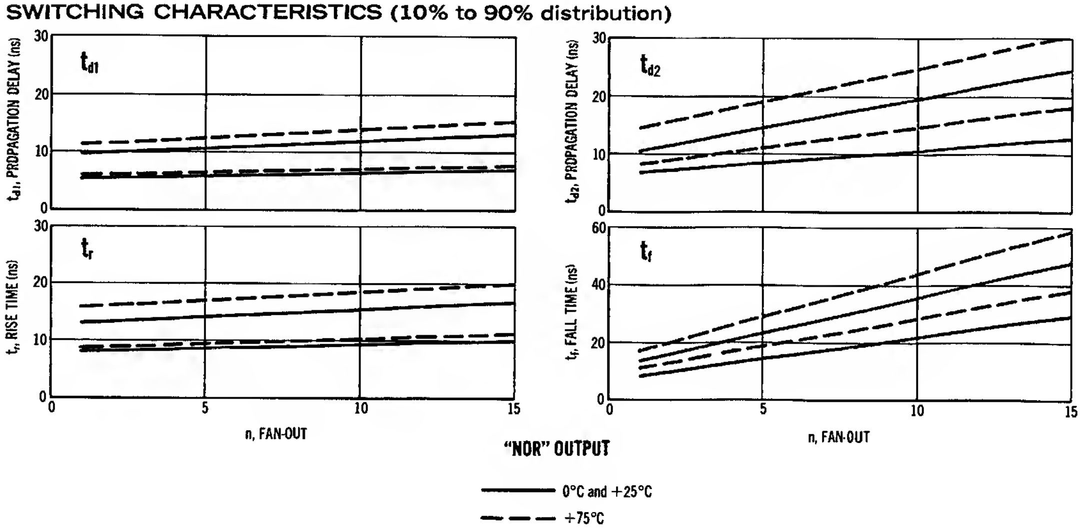
TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



SWITCHING CHARACTERISTICS (10% to 90% distribution)

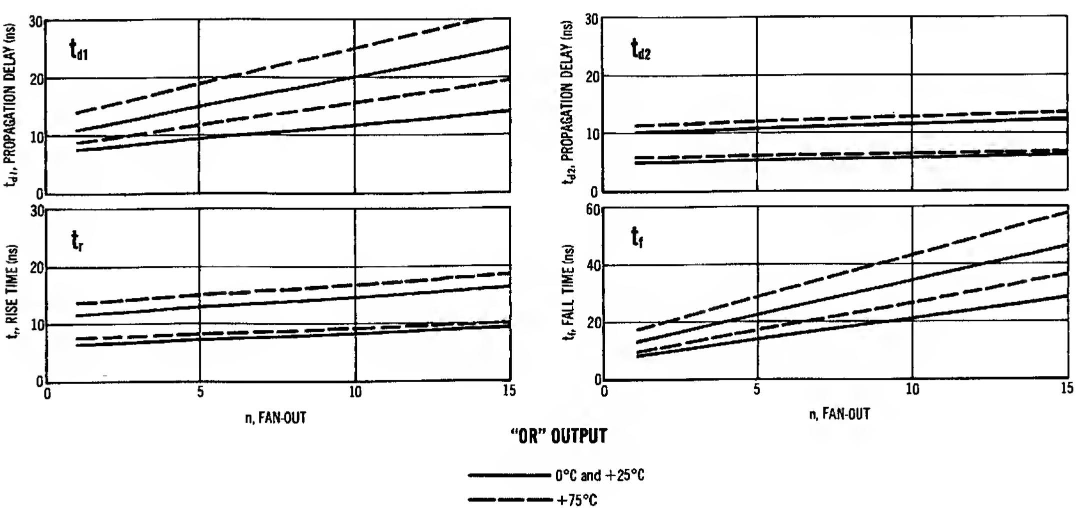


ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%				
0°C	—	−0.850	−1.350	−5.20	−1.18
+25°C	−0.670	−0.795	−1.350	−5.20	−1.15
+75°C	—	−0.725	−1.350	−5.20	−1.08

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,6,7,8,9,10	1	—	—	3	I_E (2)	—	9.25	—	8.85	—	8.15	mAdc
Input Current	6	—	—	2,7,8,9,10	1	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,6,7,8,10	1	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	2,6,7,8,9	1	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8,9,10	1	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	2,6,8,9,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7,9,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,6,7,8,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	2,6,7,8,9	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8,9,10	1	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	7	—	2,6,8,9,10	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7,9,10	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,6,7,8,10	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	2,6,7,8,9	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "1" Output Voltage	—	6	—	2,7,8,9,10	1	—	—	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	7	—	2,6,8,9,10	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7,9,10	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,6,7,8,10	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	2,6,7,8,9	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "0" Output Voltage	—	—	6	2,7,8,9,10	1	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	—	7	2,6,8,9,10	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7,9,10	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,6,7,8,10	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	2,6,7,8,9	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	—	6	2,7,8,9,10	1	—	5③	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.065	Volts
"OR" Output Voltage Change (No load to full load)	—	6	—	2,7,8,9,10	1	—	4③	3	ΔV_5 (4)	—	−0.055	—	−0.055	—	−0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8,9,10	1	6①	—	3	V_3 (5)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	2,6,8,9,10	1	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,9,10	1	8①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,8,10	1	9①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,8,9	1	10①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	4	—	2,7,8,9,10	1	—	—	3	t_{d1} (4)	9.0	12.5	9.0	12.5	9.5	16.0	ns
	6	5	—	2,7,8,9,10	1	—	—	3	t_{d1} (5)	7.0	11.0	7.0	11.0	7.5	13.0	↓
	6	4	—	2,7,8,9,10	1	—	—	3	t_{d2} (4)	6.5	11.0	6.5	11.0	7.5	13.0	↓
	6	5	—	2,7,8,9,10	1	—	—	3	t_{d2} (5)	8.5	12.5	8.5	12.5	10.0	16.0	↓
Rise Time	6	4	—	2,7,8,9,10	1	—	—	3	t_r (4)	8.0	12.0	8.0	12.0	9.5	15.5	↓
	6	5	—	2,7,8,9,10	1	—	—	3	t_r (5)	9.5	14.5	10.0	14.5	11.0	17.0	↓
Fall Time	6	4	—	2,7,8,9,10	1	—	—	3	t_f (4)	9.5	15.0	10.0	15.0	11.0	17.5	↓
	6	5	—	2,7,8,9,10	1	—	—	3	t_f (5)	9.0	15.0	9.5	15.0	10.5	17.5	↓

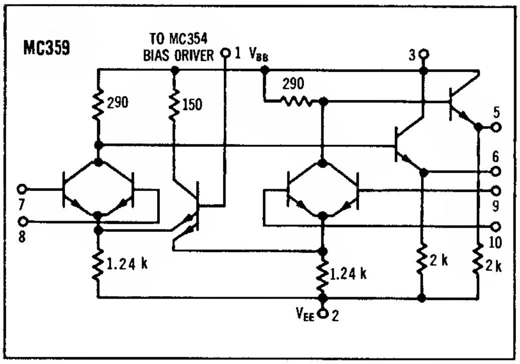
Pins not listed are left open ① Input voltage is adjusted to obtain dV "NOR/dV_{in} = "0". ③ Current test conditions: no load = 0; full load = −2.5mAdc ±5%.

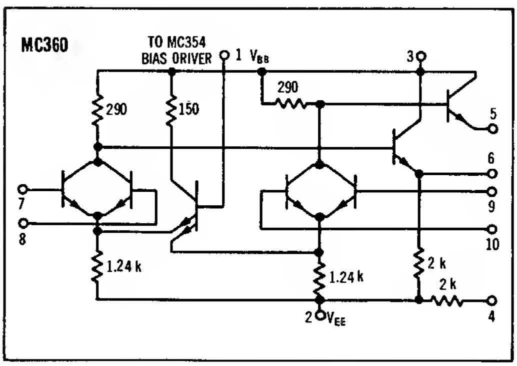


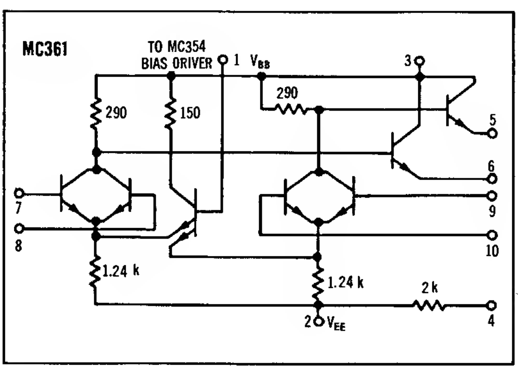
"OR" OUTPUT

MC359 • MC360 • MC361

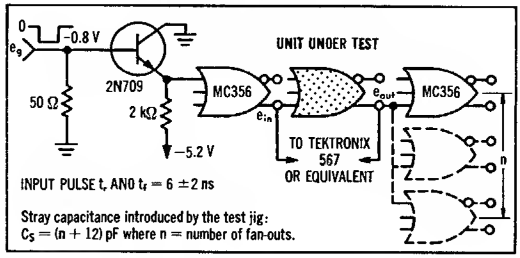
Dual 2-input gates that provide the positive logic "NOR" function. MC359 has two output pull-down resistors; MC360 has one of the output pull-down resistors optional; MC361 omits one output pull-down resistor and has the second optional.



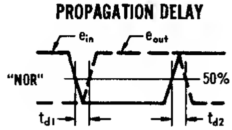




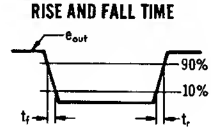
SWITCHING TIME TEST CIRCUIT



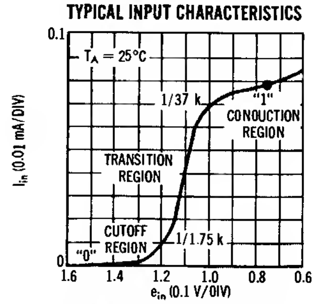
PROPAGATION DELAY



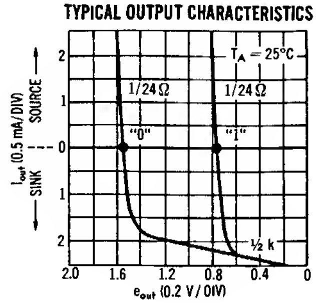
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



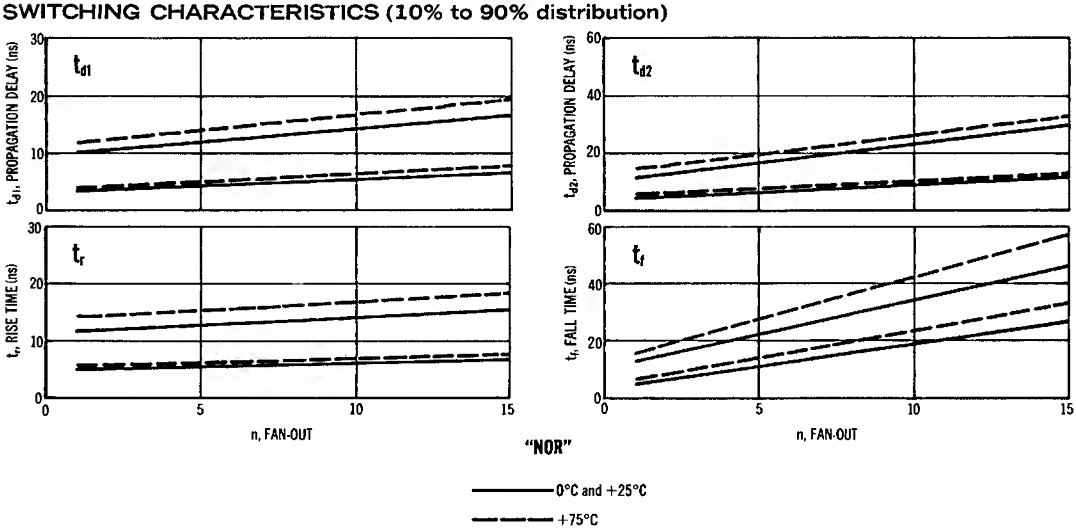
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%				
	V_H	$V_{1\,max}$	V_L	V_{EE}	V_{BB}
0°C	—	−0.850	−1.350	−5.20	−1.18
+25°C	−0.670	−0.795	−1.350	−5.20	−1.15
+75°C	—	−0.725	−1.350	−5.20	−1.08

Characteristic	V_H Pin No	$V_{1\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current MC359, MC360	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	13.55	—	13.0	—	12.0	mAdc
MC361	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	10.5	—	10.1	—	9.2	mAdc
Input Current	7	—	—	2,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	6	—	—	2,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,7,8,10	1	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	2,7,6,9	1	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	7	2,8,9,10	1	—	—	3	V_1 (6)	−0.715	−0.650	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	6	2,7,9,10	1	—	—	3	V_1 (6)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,7,6,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	2,7,8,9	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	7	—	2,6,9,10	1	—	—	3	V_0 (6)	−1.510	−1.680	−1.465	−1.750	−1.395	−1.730	Vdc
	—	6	—	2,7,9,10	1	—	—	3	V_0 (6)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,7,8,10	1	—	—	3	V_0 (5)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	2,7,8,9	1	—	—	3	V_0 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	—	—	2,7,8,9,10	1	—	6②	3	ΔV_1 (6)	—	−0.055	—	−0.055	—	−0.065	Vdc
	—	—	—	2,7,8,9,10	1	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.065	Vdc
"NOR" Saturation Breakpoint Voltage	—	—	—	2,6,9,10	1	7①	—	3	V_3 (6)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	2,7,9,10	1	8①	—	3	V_3 (6)	—	↓	—	↓	—	↓	↓
	—	—	—	2,7,8,10	1	9①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,7,6,9	1	10①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	7	6	—	2,8,9,10	1	—	—	3	t_{d1} (6)	6.5	11.0	6.5	11.0	6.0	14.5	ns
	10	5	—	2,7,8,9	1	—	—	3	t_{d1} (5)	6.5	11.0	6.5	11.0	6.0	14.5	↓
	7	6	—	2,8,9,10	1	—	—	3	t_{d2} (6)	8.5	13.5	8.5	13.5	10.0	16.0	↓
	10	5	—	2,7,6,9	1	—	—	3	t_{d2} (5)	6.5	13.5	6.5	13.5	10.0	16.0	↓
Rise Time	7	6	—	2,8,9,10	1	—	—	3	t_r (6)	8.5	12.5	9.0	12.5	11.0	15.5	↓
	10	5	—	2,7,6,9	1	—	—	3	t_r (5)	6.5	12.5	9.0	12.5	11.0	15.5	↓
Fall Time	7	6	—	2,6,9,10	1	—	—	3	t_f (6)	9.0	14.0	9.5	14.0	11.5	17.0	↓
	10	5	—	2,7,6,9	1	—	—	3	t_f (5)	9.0	14.0	9.5	14.0	11.5	17.0	↓

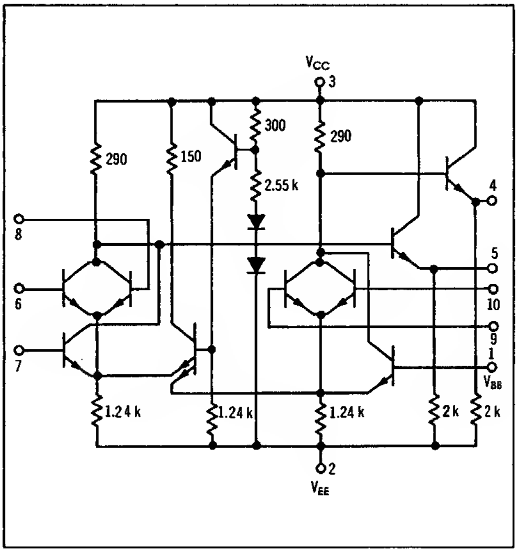
Pins not listed are left open. For MC360, connect pin 4 to pin 5 for all tests. ① Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0.
② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

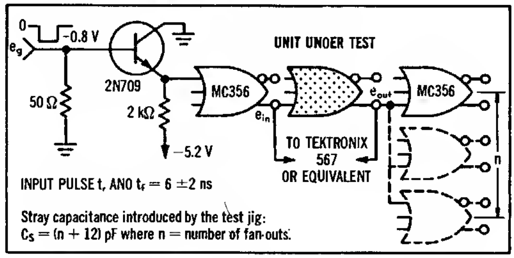


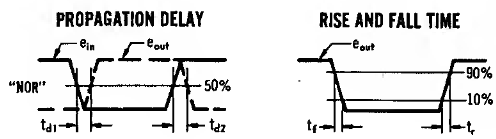
MC362A

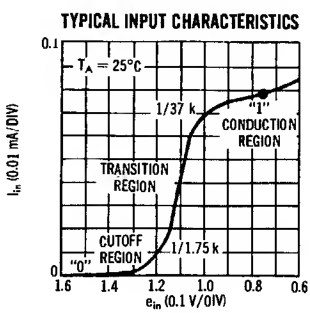
Dual 3-input gate that provides the positive logic "NOR" function, and features an internal bias driver. This gate is available without bias driver as MC362.

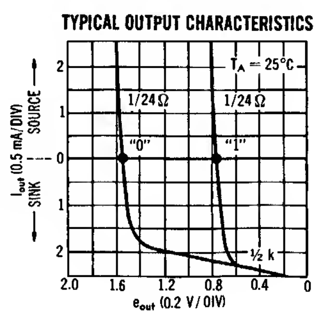


SWITCHING TIME TEST CIRCUIT









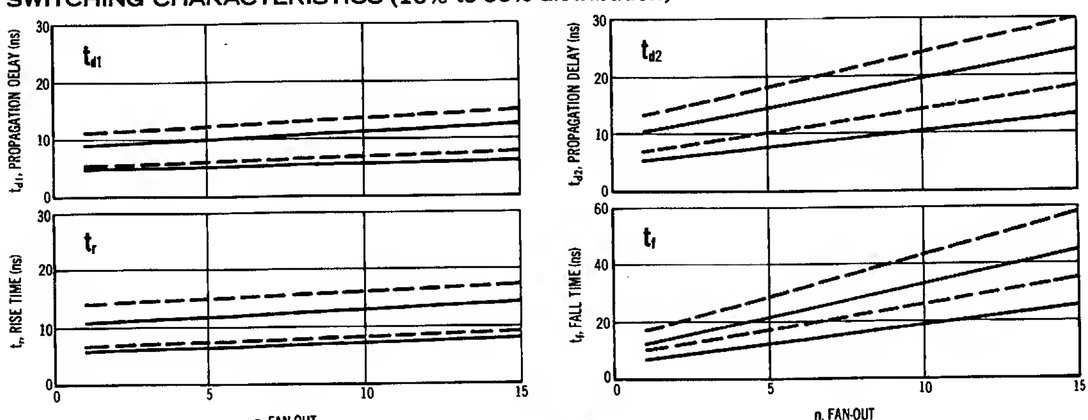
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
	V_H	$V_{I\,max}$	V_L	V_{EE}
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	1,2,6,7,8,9,10	—	—	3	I_E (2)	—	17.7	—	17.0	—	16.4	mAdc
Input Current	1	—	—	2,6,7,8,9,10	—	—	3	I_{in} (1)	—	—	—	100	—	—	μAdc
	6	—	—	1,2,7,8,9,10	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	8	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	1,2,6,8,9,10	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	1,2,6,7,9,10	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	1	2,6,7,8,9,10	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	1,2,6,7,8,10	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	1,2,6,7,8,9	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	6	—	1,2,7,8,9,10	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	7	—	1,2,6,8,9,10	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	1,2,6,7,9,10	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	1	—	2,6,7,8,9,10	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	1,2,6,7,8,10	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	1,2,6,7,8,9	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change	—	—	6	1,2,7,8,9,10	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.065	Volts
	—	—	1	2,6,7,8,9,10	—	4②	3	ΔV_1 (4)	—	−0.055	—	−0.055	—	−0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	1,2,6,8,9,10	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,9,10	8①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,8,10	9①	—	3	V_3 (4)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,8,9	10①	—	3	V_3 (4)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	1,2,7,8,9,10	—	—	3	t_{d1} (5)	6.5	10.5	6.5	10.5	7.5	11.5	ns
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d1} (4)	6.5	10.5	6.5	10.5	7.5	11.5	↓
	6	5	—	1,2,7,8,9,10	—	—	3	t_{d2} (5)	8.5	11.5	8.5	11.5	10.0	15.0	↓
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d2} (4)	8.5	11.5	8.5	11.5	10.0	15.0	↓
Rise Time	6	5	—	1,2,7,8,9,10	—	—	3	t_r (5)	9.0	12.5	9.5	12.5	11.5	15.5	↓
	1	4	—	2,6,7,8,9,10	—	—	3	t_r (4)	9.0	12.5	9.5	12.5	11.5	15.5	↓
Fall Time	6	5	—	1,2,7,8,9,10	—	—	3	t_f (5)	8.5	14.0	9.0	14.0	11.5	17.0	↓
	1	4	—	2,8,7,8,9,10	—	—	3	t_f (4)	8.5	14.0	9.0	14.0	11.5	17.0	↓

Pins not listed are left open.
① Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0. ② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

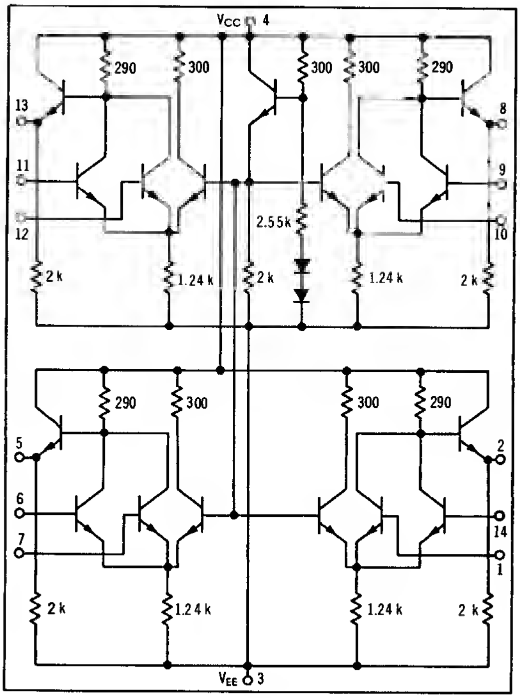


"NOR"

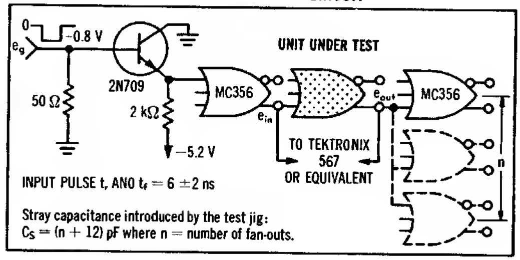
——— 0°C and +25°C
– – – +75°C

MC363F

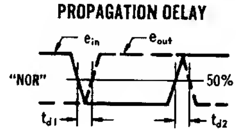
Quad 2-input gate that provides the positive logic "NOR" function, and features an internal bias driver.



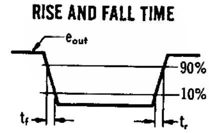
SWITCHING TIME TEST CIRCUIT



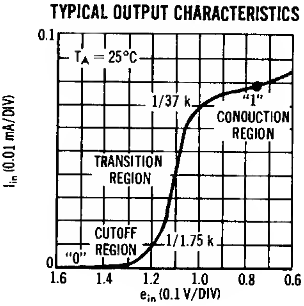
PROPAGATION DELAY



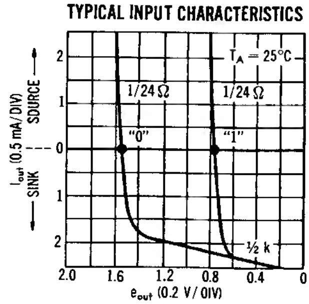
RISE AND FALL TIME



TYPICAL OUTPUT CHARACTERISTICS



TYPICAL INPUT CHARACTERISTICS



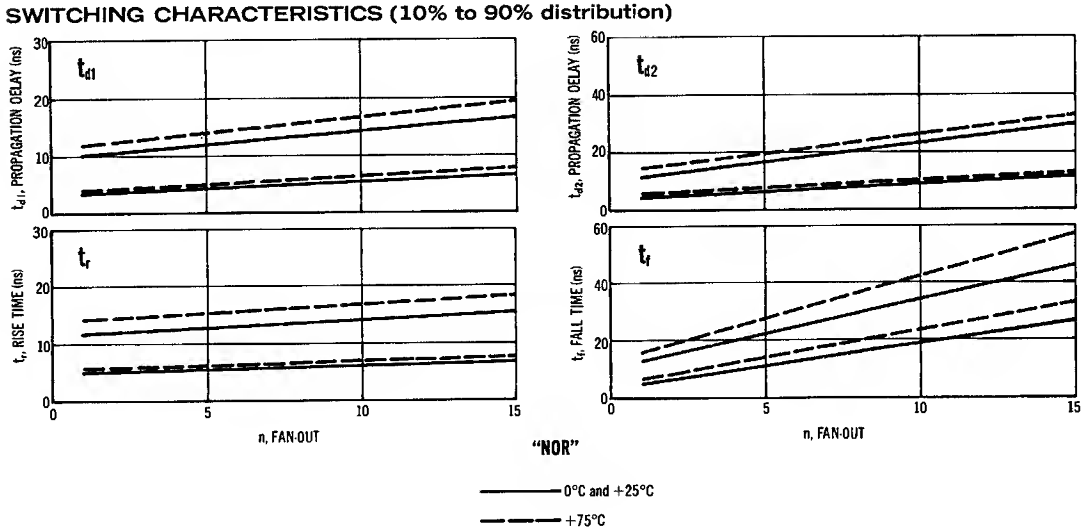
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ± 1%: V_H	$V_{I\,max}$	V_L	V_{EE}
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No In ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	1,3,6,7,9,10,11,12,14	—	—	4	I_E (3)	—	31.0	—	30.0	—	29.0	mAdc
Input Current	1	—	—	3,6,7,9,10,11,12,14	—	—	4	I_{in} (1)	—	—	—	100	—	—	μAdc
	6	—	—	1,3,7,9,10,11,12,14	—	—	4	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,3,6,9,10,11,12,14	—	—	4	I_{in} (7)	—	—	—	↓	—	—	↓
	9	—	—	1,3,6,7,10,11,12,14	—	—	4	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	1 3,6,7,9,11,12,14	—	—	4	I_{in} (10)	—	—	—	↓	—	—	↓
	11	—	—	1 3,6,7,9,10,12,14	—	—	4	I_{in} (11)	—	—	—	↓	—	—	↓
	12	—	—	1,3,6,7,9,10,11,14	—	—	4	I_{in} (12)	—	—	—	↓	—	—	↓
	14	—	—	1,3,6,7,9 10,11,12	—	—	4	I_{in} (14)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	1	3,6,7,9,10,11,12,14	—	—	4	V_1 (2)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	6	1,3,7,9,10,11,12,14	—	—	4	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	7	1,3,6,9,10,11,12,14	—	—	4	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	1,3,6,7,10,11,12,14	—	—	4	V_1 (8)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	1,3,6,7,9,11,12,14	—	—	4	V_1 (8)	↓	↓	↓	↓	↓	↓	↓
	—	—	11	1,3,6,7,9,10,12,14	—	—	4	V_1 (13)	↓	↓	↓	↓	↓	↓	↓
	—	—	12	1,3,6,7,9,10,11,14	—	—	4	V_1 (13)	↓	↓	↓	↓	↓	↓	↓
	—	—	14	1,3,6,7,9,10,11,12	—	—	4	V_1 (2)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	1	—	3,6,7,9,10,11,12,14	—	—	4	V_4 (2)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	6	—	1,3 7,9,10,11,12,14	—	—	4	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	7	—	1,3,6,9,10,11,12,14	—	—	4	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	1,3 6,7,10,11,12,14	—	—	4	V_4 (8)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	1,3,6,7,9,11,12,14	—	—	4	V_4 (8)	↓	↓	↓	↓	↓	↓	↓
	—	11	—	1,3,6,7,9,10,12,14	—	—	4	V_4 (13)	↓	↓	↓	↓	↓	↓	↓
	—	12	—	1,3,6,7,9,10,11,14	—	—	4	V_4 (13)	↓	↓	↓	↓	↓	↓	↓
	—	14	—	1,3,6,7,9,10,11,12	—	—	4	V_4 (2)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	—	—	1,3,6,7,9,10,11,12,14	—	2②	4	ΔV_1 (2)	—	−0.055	—	−0.055	—	−0.065	Volts
	—	—	—	1,3,6,7,9,10,11,12,14	—	5②	4	ΔV_1 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	—	8②	4	ΔV_1 (8)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	—	13②	4	ΔV_1 (13)	—	↓	—	↓	—	↓	↓
"NOR" Saturation Breakpoint Voltage	—	—	—	3,6,7,9,10,11,12,14	1①	—	4	V_3 (2)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	1,3,6,9,10,11,12,14	7①	—	4	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,11,12,14	10①	—	4	V_3 (8)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,14	12①	—	4	V_3 (13)	—	↓	—	↓	—	↓	↓
Switching Time	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_{d1} (2)	6.5	11.0	6.5	11.0	8.0	14.5	ns
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_{d1} (5)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_{d1} (8)	↓	↓	↓	↓	↓	↓	↓
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_{d1} (13)	↓	↓	↓	↓	↓	↓	↓
	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_{d2} (2)	8.5	13.5	8.5	13.5	10.0	16.0	↓
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_{d2} (5)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_{d2} (8)	↓	↓	↓	↓	↓	↓	↓
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_{d2} (13)	↓	↓	↓	↓	↓	↓	↓
Rise Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_r (2)	8.5	12.5	9.0	12.5	11.0	15.5	↓
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_r (5)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_r (8)	↓	↓	↓	↓	↓	↓	↓
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_r (13)	↓	↓	↓	↓	↓	↓	↓
Fall Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_f (2)	9.0	14.0	9.5	14.0	11.5	17.0	↓
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_f (5)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_f (8)	↓	↓	↓	↓	↓	↓	↓
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_f (13)	↓	↓	↓	↓	↓	↓	↓

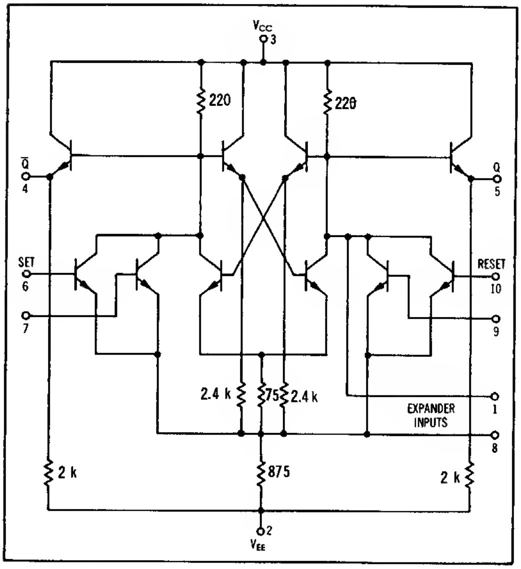
Pins not listed are left open. ① Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0. ② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

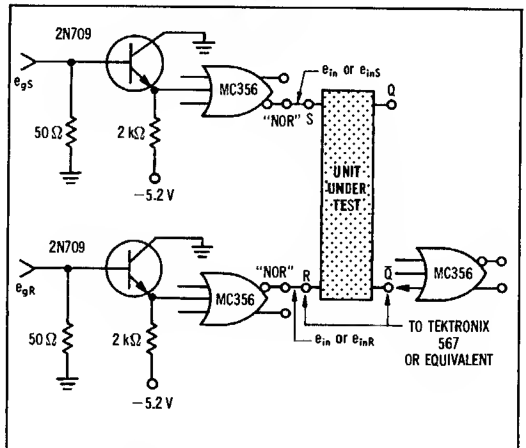


MC352A

DC Set-Reset flip-flop with an expandable input and buffered outputs. This flip-flop is available without buffered outputs as MC352.

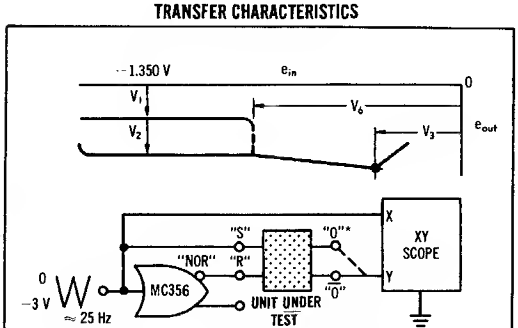


SWITCHING TIME TEST CIRCUIT



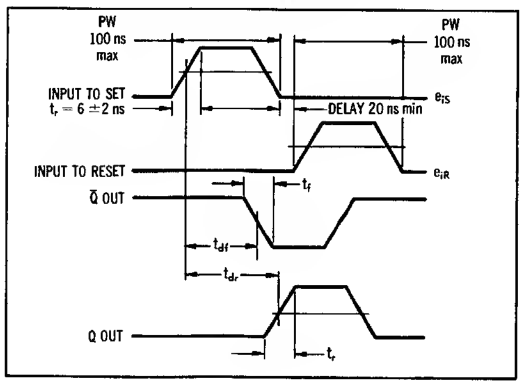
Stray capacitance introduced by the test jig:
$C_S = (n + 12)$ pF where n = number of fan-outs.

TRANSFER CHARACTERISTICS



*FOR "0" TESTS REVERSE "S" AND "R" CONNECTIONS

SWITCHING TIME WAVEFORMS



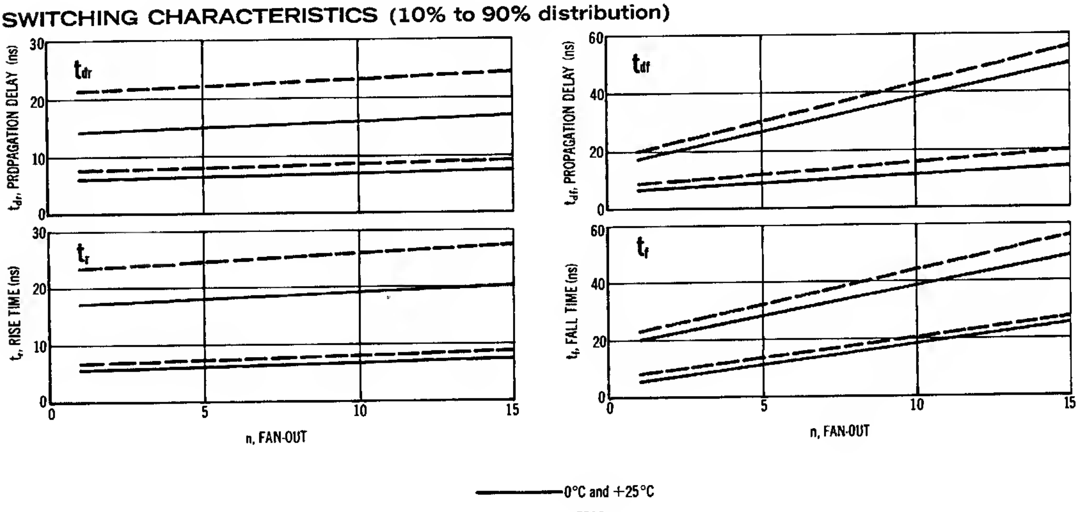
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L③ Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,6,7,9,10	—	—	3	I_E (6)	—	10.35	—	10.35	—	9.52	mAdc
Input Current	6	—	—	2,7,9,10	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,9,10	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	9	—	—	2,6,7,10	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	2,6,7,9	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"Q" Logical "1" Output Voltage	—	—	6	2,7,9,10	—	—	3	V_1 (5)	−0.715	−0.650	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	2,6,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"Q" Logical "0" Output Voltage	—	—	9	2,6,7,10	—	—	3	V_2 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	—	10	2,6,7,9	—	—	3	V_2 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"$\bar{Q}$" Logical "1" Output Voltage	—	—	9	2,6,7,10	—	—	3	V_1 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	10	2,6,7,9	—	—	3	V_1 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	—	—	6	2,7,9,10	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	—	7	2,6,9,10	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"Q" Output Voltage Change	—	6	—	2,7,9,10	—	5②	3	ΔV_1 (5)	—	−0.065	—	−0.065	—	−0.075	Volts
"$\bar{Q}$" Output Voltage Change	—	10	—	2,6,7,9	—	4②	3	ΔV_1 (4)	—	−0.065	—	−0.065	—	−0.075	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	2,7,9	6,10①	—	3	V_3 (5)	—	−0.61	—	−0.65	—	−0.73	Vdc
"$\bar{Q}$" Saturation Breakpoint Voltage	—	—	—	2,7,9	6,10①	—	3	V_3 (4)	—	−0.61	—	−0.65	—	−0.73	Vdc
"Q" or "$\bar{Q}$" Latch Voltage	—	—	—	2,7,9	6,10④	—	3	V_6 (6,10)	−1.11	−1.25	−1.09	−1.21	−1.02	−1.14	Vdc
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6,10	4,5	—	2,7,9	—	—	3	t_{dr} (4,5)	10.0	16.0	10.5	16.0	13.5	22.0	ns
	6,10	4,5	—	2,7,9	—	—	3	t_{df} (4,5)	11.0	19.5	11.5	19.5	14.0	22.0	↓
Rise Time	6,10	4,5	—	2,7,9	—	—	3	t_r (4,5)	11.0	19.0	11.5	19.0	13.5	26.0	↓
Fall Time	6,10	4,5	—	2,7,9	—	—	3	t_f (4,5)	12.0	19.5	12.5	19.5	14.0	26.0	↓

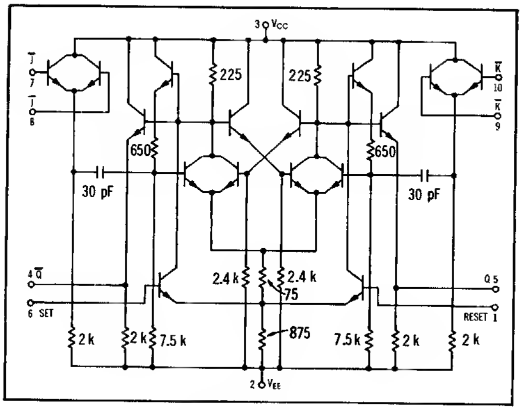
Pins not listed are left open. ① Input voltage is adjusted to obtain dV "Q"/dV_{in} = 0; dV "$\bar{Q}$"/dV_{in} = 0. ② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.
③ Apply momentary $V_{I\,max}$ to set output, then V_L for measurement. ④ Input voltage is adjusted to obtain $dV_1/dV_{in} \approx \infty$.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



MC358A

AC-coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.



TRANSFER CHARACTERISTICS

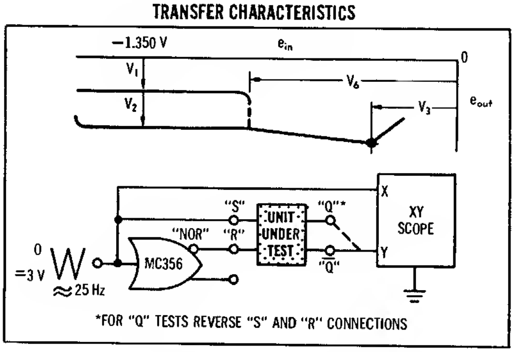


FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

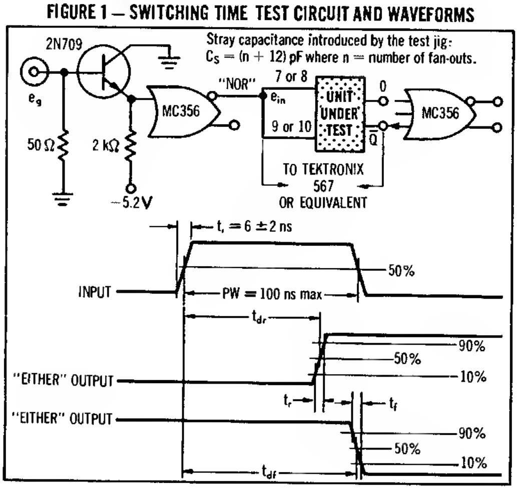


FIGURE 2 — INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

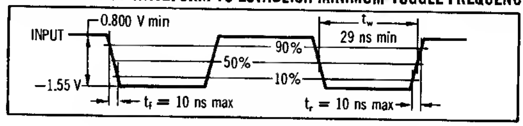


FIGURE 3 — SENSITIVITY (NO TOGGLE)

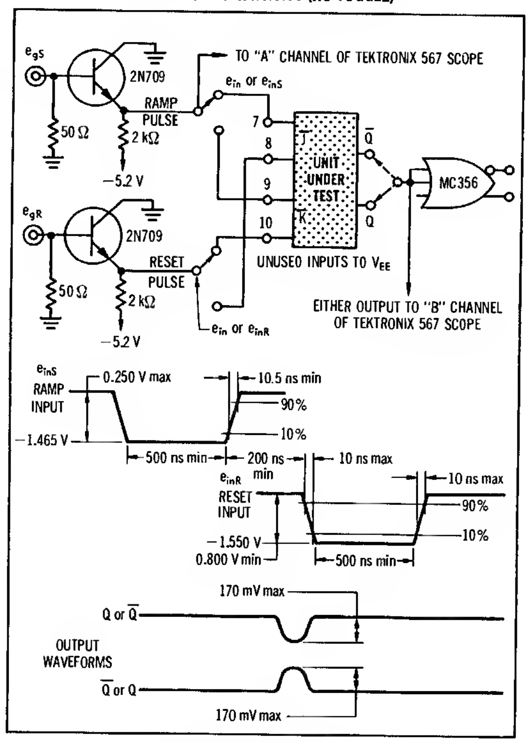
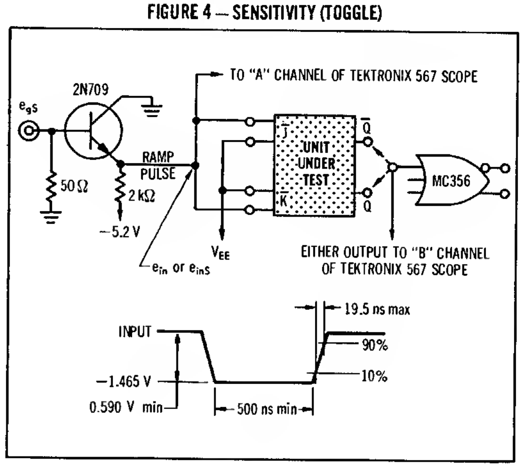


FIGURE 4 — SENSITIVITY (TOGGLE)



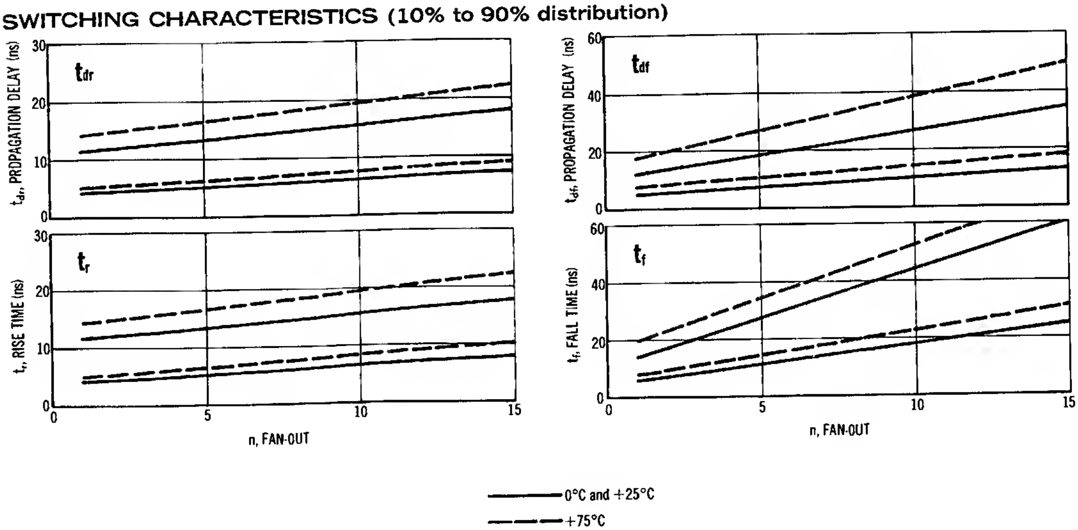
ELECTRICAL CHARACTERISTICS

@ Test Temperature	V_H	$V_{I\,max}$	V_L	V_{EE}
	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L③ Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	7,10	—	1,2,8,8,9	—	—	3	I_E (2)	—	22.0	—	21.0	—	19.6	mAdc
Input Current	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	100	—	—	µAdc
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,8,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	8	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"Q" Logical "0" Output Voltage	—	—	1	2,8,7,8,9,10	—	—	3	V_2 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"$\overline{Q}$" Logical "1" Output Voltage	—	—	1	2,6,7,8,9,10	—	—	3	V_1 (4)	−0.715	−0.850	−0.870	−0.795	−0.590	−0.725	Vdc
"$\overline{Q}$" Logical "0" Output Voltage	—	—	6	1,2,7,8,9,10	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"Q" Output Voltage Change	—	6	—	1,2,7,8,9,10	—	5②	3	ΔV_1 (5)	—	−0.065	—	−0.085	—	−0.075	Volts
"$\overline{Q}$" Output Voltage Change	—	1	—	2,8,7,8,9,10	—	4②	3	ΔV_1 (4)	—	−0.065	—	−0.065	—	−0.075	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.81	—	−0.85	—	−0.73	Vdc
"$\overline{Q}$" Saturation Breakpoint Voltage	—	—	—	2,8,7,8,9,10	1①	—	3	V_3 (4)	—	−0.61	—	−0.85	—	−0.73	Vdc
"Q" or "$\overline{Q}$" Latch Voltage	—	—	—	2,7,8,9,10	1,8④	—	3	V_4 (1,6)	−1.11	−1.25	−1.09	−1.21	−1.02	−1.14	Vdc
	Pulse In	Pulse Out													
Toggle Frequency (See Figures 1 and 2)	7,10	5		1,2,6,9	—	—	3	f_{Tog}	—	—	15	—	—	—	MHz
Sensitivity (No Toggle)	7,10	4		1,2,8,8,9	—	—	3		See Figure 3						
	8,9	5		1,2,6,7,10	—	—	3		See Figure 3						
Sensitivity (Toggle)	7,10	4,5		1,2,6,8,9	—	—	3		See Figure 4						
									Typ	Max	Typ	Max	Typ	Max	
Switching Times Propagation Delay	7,10	4,5		1,2,8,8,9	—	—	3	t_{dr} (4,5)	7.5	13.0	7.5	13.0	8.0	18.0	ns
	7,10	4,5		1,2,6,8,9	—	—	3	t_{df} (4,5)	10.0	14.5	10.0	15.0	11.0	20.0	↓
Rise Time	7,10	4,5		1,2,8,8,9	—	—	3	t_r (4,5)	8.0	13.0	8.0	13.0	8.5	16.0	
Fall Time	7,10	4,5		1,2,6,8,9	—	—	3	t_f (4,5)	10.5	15.5	11.0	15.5	12.5	22.0	

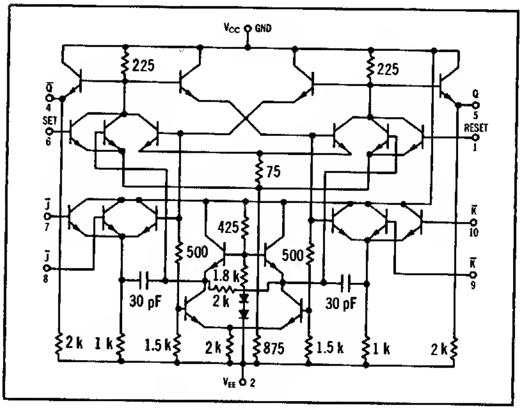
Pins not listed are left open. ① Input voltage is adjusted to obtain dV_{out}/dV_{in} = "0". ② Current test conditions: no load = 0 to full load = −2.5 mAdc ±5%.
③ Apply momentary $V_{I\,max}$ to set output, then V_{in} for measurement. ④ Input voltage is adjusted to obtain $dV_1/dV_{in} = \infty$.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

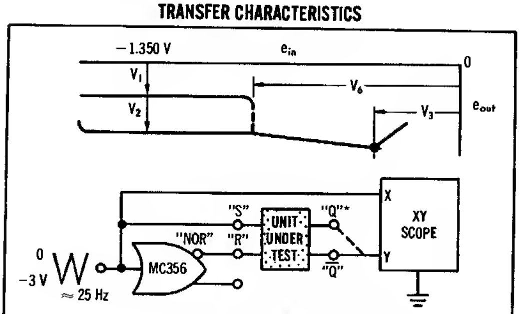


MC364

High-speed ac-coupled J-K flip-flop with dc Set and Reset input for counter and shift register applications up to 30 MHz operation.



TRANSFER CHARACTERISTICS



*FOR "Q" TESTS REVERSE "S" AND "R" CONNECTIONS

FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

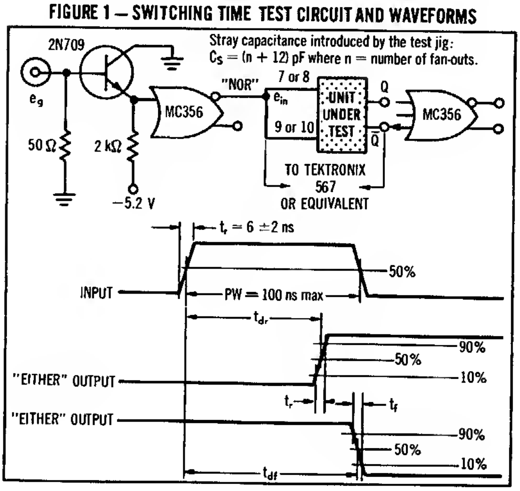


FIGURE 2 — INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

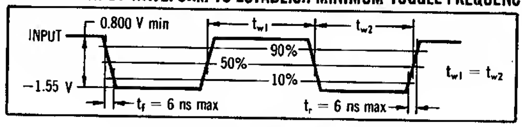


FIGURE 3 — SENSITIVITY (NO TOGGLE)

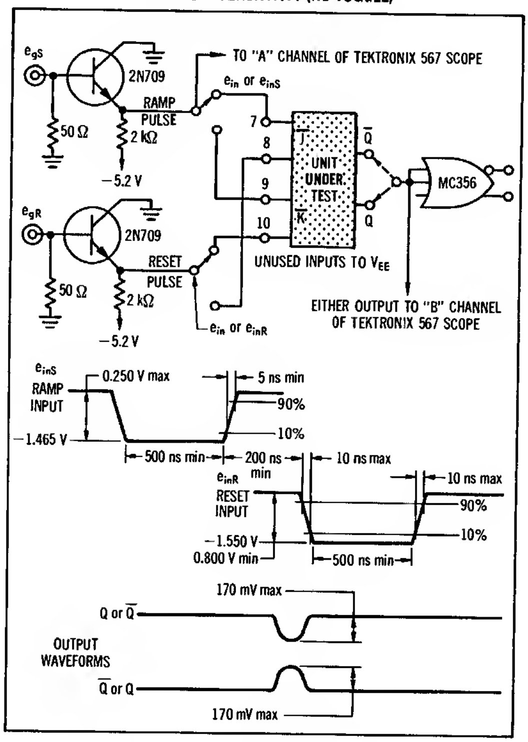
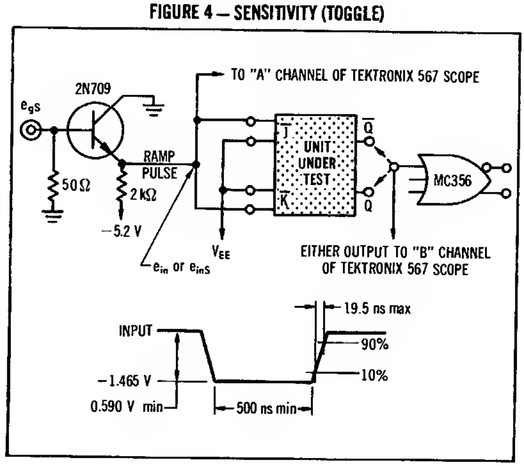


FIGURE 4 — SENSITIVITY (TOGGLE)



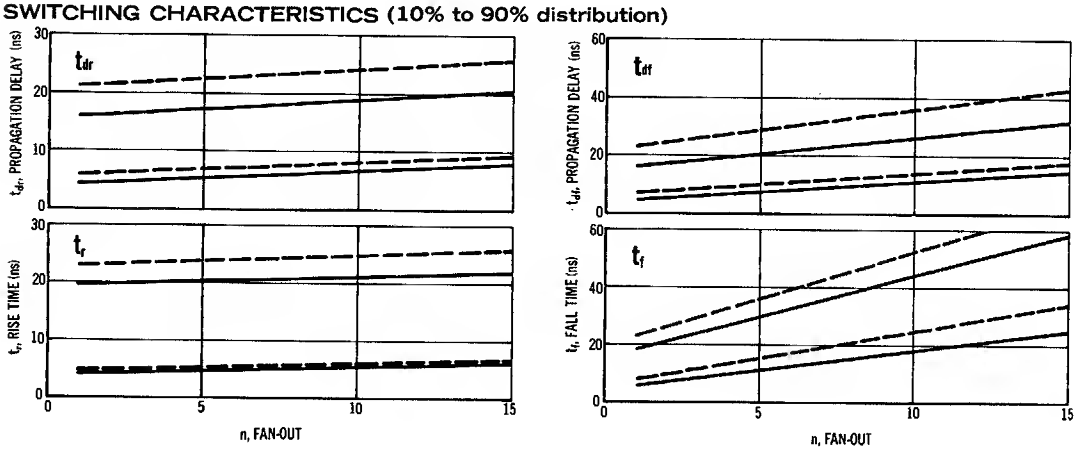
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
	V_H	$V_{I\,max}$	V_L	V_{EE}
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	7,10	—	1,2,8,8,9	—	—	3	I_E (2)	—	30.0	—	28.5	—	28.0	mAdc
Input Current	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	100	—	—	µAdc
	8	—	—	1,2,8,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,8,7,8,10	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	1,2,8,7,8,9	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"Q" Logical "1" Output Voltage	—	—	8③	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"Q" Logical "0" Output Voltage	—	—	1③	2,8,7,8,9,10	—	—	3	V_2 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"$\bar{Q}$" Logical "1" Output Voltage	—	—	1③	2,8,7,8,9,10	—	—	3	V_1 (4)	−0.715	−0.850	−0.870	−0.795	−0.590	−0.725	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"Q" Output Voltage Change	—	6	—	1,2,7,8,9,10	—	5②	3	ΔV_1 (5)	—	−0.085	—	−0.065	—	−0.075	Volts
"$\bar{Q}$" Output Voltage Change	—	1	—	2,8,7,8,9,10	—	4②	3	ΔV_1 (4)	—	−0.065	—	−0.065	—	−0.075	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.81	—	−0.65	—	−0.73	Vdc
"$\bar{Q}$" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—	−0.61	—	−0.85	—	−0.73	Vdc
"Q" or "$\bar{Q}$" Latch Voltage	—	—	—	2,7,8,9,10	1,8④	—	3	V_4 (1,8)	−1.11	−1.25	−1.09	−1.21	−1.02	−1.14	Vdc
	Pulse In	Pulse Out													
Toggle Frequency (See Figures 1 and 2)	7,10	5	—	1,2,8,9	—	—	3	f_{Tog}	—	—	30	—	—	—	MHz
Sensitivity (No Toggle)	7,10	4	—	1,2,6,8,9	—	—	3	← See Figure 3 →							
	8,9	5	—	1,2,6,7,10	—	—	3	← See Figure 3 →							
Sensitivity (Toggle)	7,10	4,5	—	1,2,8,8,9	—	—	3	← See Figure 4 →							
Switching Times									Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	7,10	4,5	—	1,2,8,8,9	—	—	3	t_{dr} (4,5)	11.0	18.0	12.0	18.0	14.0	24.0	ns
	7,10	4,5	—	1,2,8,8,9	—	—	3	t_{df} (4,5)	12.0	18.0	13.0	18.0	15.0	24.0	↓
Rise Time	7,10	4,5	—	1,2,8,8,9	—	—	3	t_r (4,5)	11.5	20.0	12.5	21.0	15.0	28.0	↓
Fall Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_f (4,5)	11.5	18.0	12.5	21.0	15.0	28.0	↓

Pins not listed are left open.
① Input voltage is adjusted to obtain $dV_{out}/dV_{in} = 0$.
② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.
③ Apply momentary $V_{I\,max}$ to set output, then V_{in} for measurement.
④ Input voltage is adjusted to obtain $dV_1/dV_{in} = \infty$.

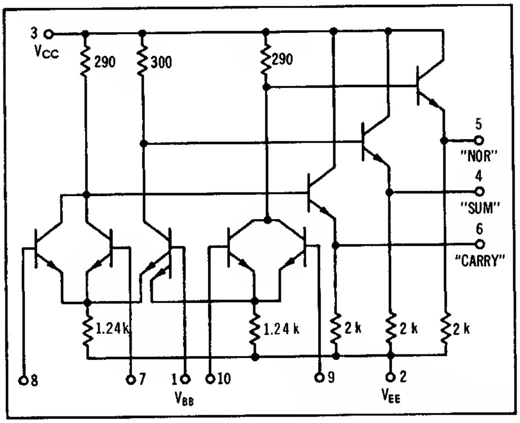
SWITCHING CHARACTERISTICS (10% to 90% distribution)



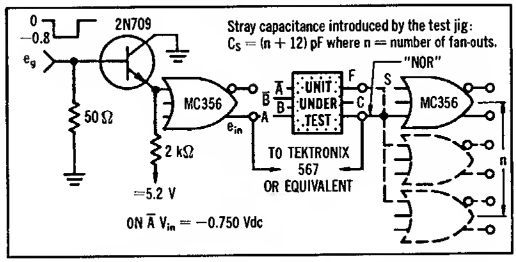
——— 0°C and +25°C
— — — +75°C

MC353

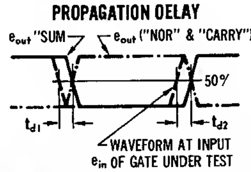
Half-adder that provides the "SUM", "CARRY", and "NOR" functions simultaneously.



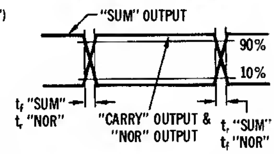
SWITCHING TIMES TEST CIRCUIT



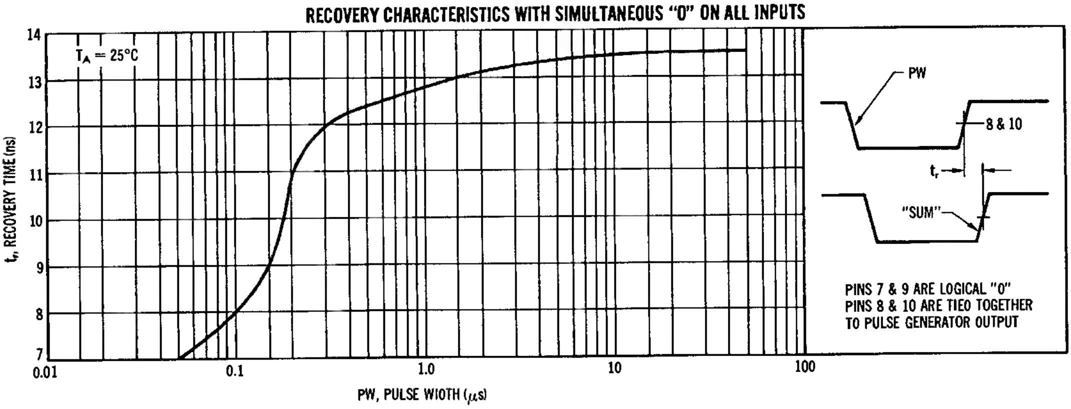
PROPAGATION DELAY



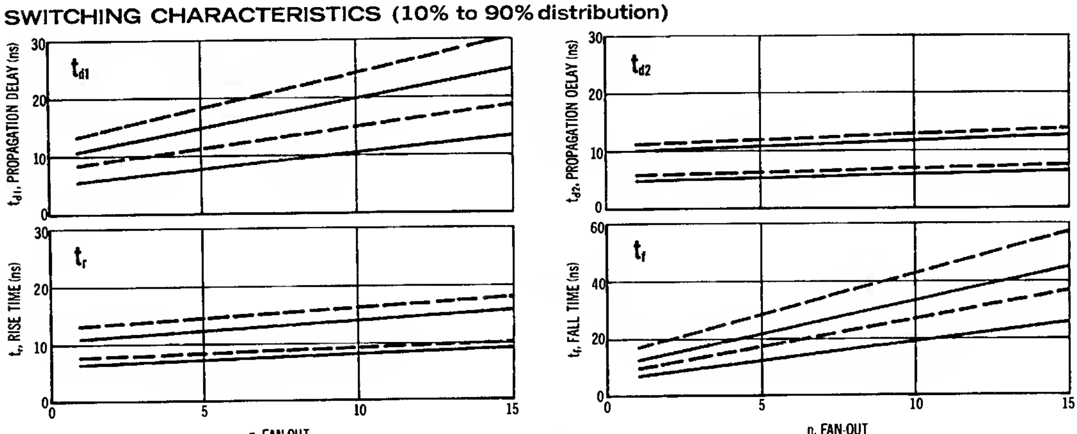
RISE AND FALL TIMES



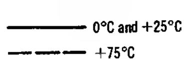
RECOVERY CHARACTERISTICS WITH SIMULTANEOUS "0" ON ALL INPUTS



SWITCHING CHARACTERISTICS (10% to 90% distribution)



"SUM"



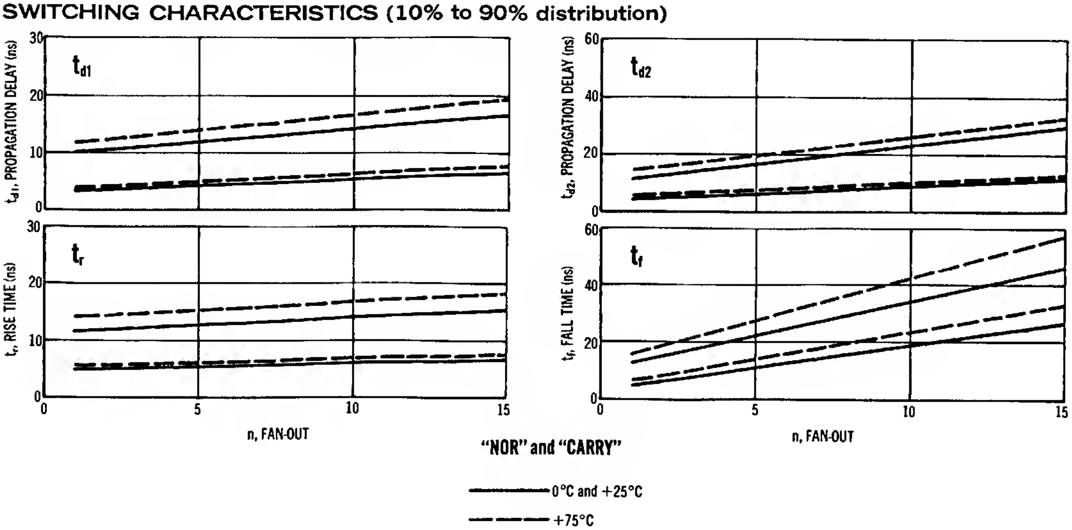
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1% V_H	$V_{I\,max}$	V_L	V_{EE}	V_{BB}
0°C	—	−0.850	−1.350	−5.20	−1.18
+25°C	−0.670	−0.795	−1.350	−5.20	−1.15
+75°C	—	−0.725	−1.350	−5.20	−1.08

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	15.9	—	15.3	—	14.1	mAdc
Input Current	7	—	—	2,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	100	—	—	µAdc
	8	—	—	2,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,7,8,10	1	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	2,7,8,9	1	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	9	2,7,8,10	1	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	10	2,7,8,9	1	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"NOR" Logical "0" Output Voltage	—	9	—	2,7,8,10	1	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	10	—	2,7,8,9	1	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"CARRY" Logical "1" Output Voltage	—	—	7	2,8,9,10	1	—	—	3	V_1 (6)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	8	2,7,9,10	1	—	—	3	V_1 (6)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"CARRY" Logical "0" Output Voltage	—	7	—	2,8,9,10	1	—	—	3	V_4 (6)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	8	—	2,7,9,10	1	—	—	3	V_4 (6)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"SUM" Logical "1" Output Voltage	—	7,9	—	2,8,10	1	—	—	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	8,10	—	2,7,9	1	—	—	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"SUM" Logical "0" Output Voltage	—	7	10	2,8,9	1	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	8	10	2,7,9	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	8	2,7,10	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	10	7	2,8,9	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	10	—	2,7,8,9	1	—	5②	3	ΔV_1 (5)	—	0.055	—	0.055	—	0.065	Volts
"CARRY" Output Voltage Change (No load to full load)	—	—	7	2,8,9,10	1	—	6②	3	ΔV_1 (6)	—	0.055	—	0.055	—	0.065	Volts
"SUM" Output Voltage Change (No load to full load)	—	7,10	—	2,8,9	1	—	4②	3	ΔV_5 (4)	—	0.055	—	0.055	—	0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8,9	1	10①	—	3	V_3 (5)	—	0.510	—	0.550	—	0.630	Vdc
"CARRY" Saturation Breakpoint Voltage	—	—	—	2,8,9,10	1	7①	—	3	V_3 (6)	—	0.510	—	0.550	—	0.630	Vdc
Switching Times						Pulse In	Pulse Out			Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	—	—	—	2,7,8,9	1	10	5	3	t_{d1} (5)	6.5	11.0	6.5	11.0	7.0	13.0	ns
	—	—	—	2,8,9,10	1	7	6	3	t_{d1} (6)	6.5	11.0	6.5	11.0	7.0	13.0	↓
	—	7	—	2,8,9	1	10	4	3	t_{d1} (4)	8.5	11.5	8.5	11.5	10.0	15.0	↓
	—	—	—	2,7,8,9	1	10	5	3	t_{d2} (5)	8.5	13.5	8.5	13.5	10.0	16.0	↓
	—	—	—	2,8,9,10	1	7	6	3	t_{d2} (6)	8.5	13.5	8.5	13.5	10.0	16.0	↓
	—	7	—	2,8,9	1	10	4	3	t_{d2} (4)	6.0	11.0	6.0	11.0	7.5	12.0	↓
Rise Time	—	—	—	2,7,8,9	1	10	5	3	t_r (5)	9.0	12.5	9.0	12.5	11.0	15.5	↓
	—	—	—	2,8,9,10	1	7	6	3	t_r (6)	9.0	12.5	9.0	12.5	11.0	15.5	↓
	—	7	—	2,8,9	1	10	4	3	t_r (4)	7.0	11.5	7.0	11.5	9.0	13.0	↓
Fall Time	—	—	—	2,7,8,9	1	10	5	3	t_f (5)	9.0	14.0	9.5	14.0	11.5	17.0	↓
	—	—	—	2,8,9,10	1	7	6	3	t_f (6)	9.0	14.0	9.5	14.0	11.5	17.0	↓
	—	7	—	2,8,9	1	10	4	3	t_f (4)	9.0	14.0	9.5	14.0	12.0	17.0	↓

Pins not listed are left open. ① Input voltage is adjusted to obtain dV"NOR"/dV_{in} = 0 or dV "CARRY"/dV_{in} = 0.
② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

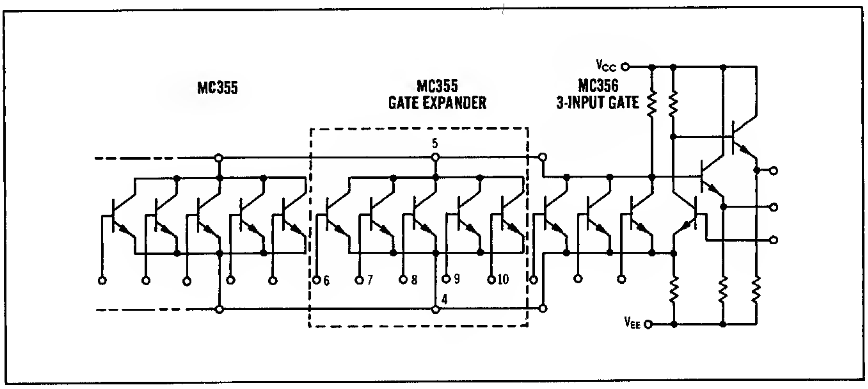
SWITCHING CHARACTERISTICS (10% to 90% distribution)



"NOR" and "CARRY"

MC355

A 5-input expander for use with the MC352A, MC356, MC357, and MC365. Each expander unit increases the fan-in of the basic gate by five.

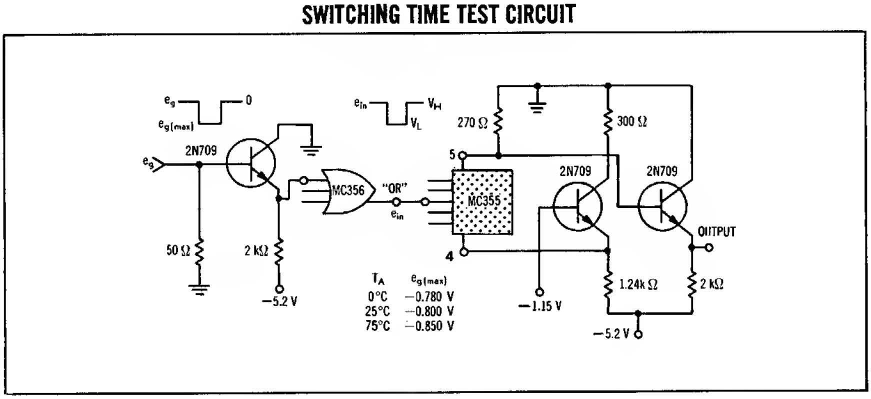


ELECTRICAL CHARACTERISTICS

Characteristic	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	V_{CB} Pin No	V_{BE} Pin No	I_E Pin No	Ground Pin No	Symbol Pin No in ( )	0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Test Conditions (Vdc ±1%; I_E mAdc) @ Test Temperature 0°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33									
+25°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33									
+75°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33									
Base Leakage Current	4	6	—	—	—	—	5	I_{BL} (6)	—	0.5	—	0.5	—	2.0	μAdc
	4	7	—	—	—	—	5	I_{BL} (7)	—	↓	—	↓	—	↓	↓
	4	8	—	—	—	—	5	I_{BL} (8)	—	↓	—	↓	—	↓	↓
	4	9	—	—	—	—	5	I_{BL} (9)	—	↓	—	↓	—	↓	↓
	4	10	—	—	—	—	5	I_{BL} (10)	—	↓	—	↓	—	↓	↓
Collector Leakage Current	—	—	5	—	6,7,8,9,10	—	4	I_{CEX} (5)	—	1.0	—	1.0	—	15.0	μAdc
Input Voltage	—	—	—	5	—	4	6	V_{BE} (4)	0.730	0.780	0.680	0.730	0.580	0.630	Vdc
	—	—	—	5	—	4	7	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	8	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	9	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	10	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
Switching Times	Pulse In / Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	8 / ①	—	—	—	—	—	—	t_{d1}	4.5	9.5	4.5	9.5	5.5	13.0	ns
	8 / ①	—	—	—	—	—	—	t_{d2}	4.0	9.0	4.0	9.0	4.5	12.0	↓
Rise Time	8 / ①	—	—	—	—	—	—	t_r	8.5	13.0	8.5	13.0	9.0	15.0	↓
Fall Time	8 / ①	—	—	—	—	—	—	t_f	3.5	10.5	3.5	10.5	4.0	11.5	↓

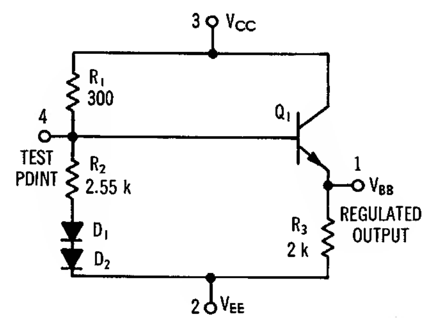
Pins not listed are left open. ①See Switching Time Test Circuit.

SWITCHING TIME TEST CIRCUIT



MC354

Bias driver that compensates for changes in circuit parameters with temperature.



ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%
0°C	−5.20
+25°C	−5.20
+75°C	−5.20

Characteristic	V_{EE} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	2	—	3	I_E (2)	—	4.6	—	4.4	—	4.0	mAdc
Output Voltage	2	1①	3	V_{BB}	−1.14	−1.27	−1.09	−1.22	−1.04	−1.18	Vdc

Pins not listed are left open.

① Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

CIRCUIT DESCRIPTION

Circuit Operation:

The divider network R_1, R_2, D_1, D_2 compensates for temperature variations of the base-emitter voltages of Q_1, and of the driven gates, producing a bias voltage for the MECL logic circuits that maintains a constant set of dc operating conditions over the temperature range of 0 to +75°C. In addition, compensation for power supply variations is achieved, since the bias output voltage is derived from the system supply.

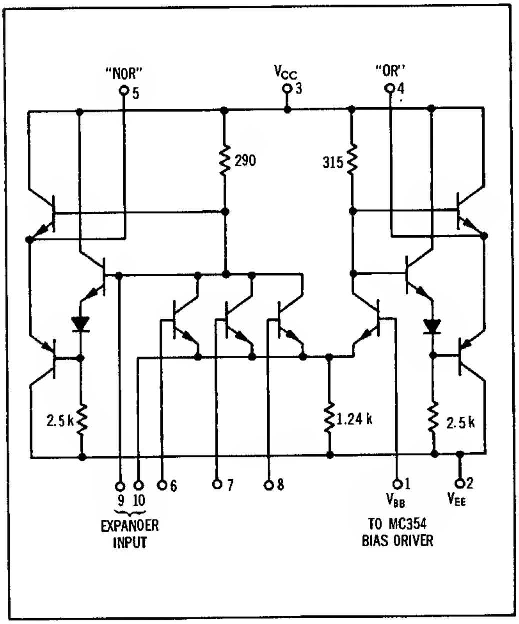
Either of the supply voltage nodes may be used as ground, however the ground potential of the bias driver must coincide with that of the logic system. Thus, if V_{CC} is grounded in the logic system, then —

$V_{CC} = 0$; $V_{EE} = -5.2$ V;

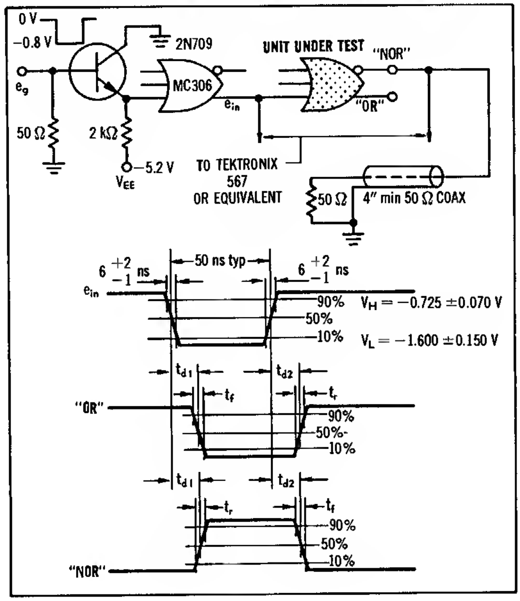
$V_{BB} = -1.15$ nominal output voltage at 25°C

MC365

Line driver for driving lines of 50 ohms or greater while providing the positive logic "NOR" function and its complement simultaneously.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



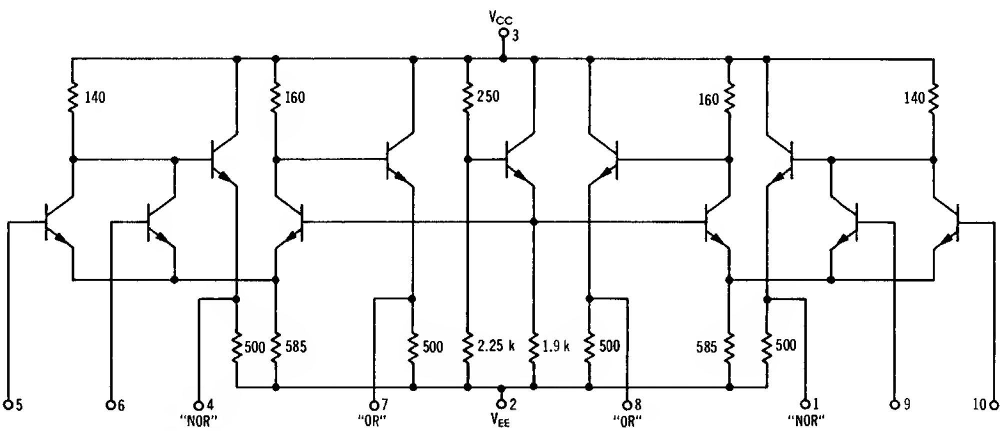
ELECTRICAL CHARACTERISTICS

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	I_L ① Pin No	Ground Pin No	Symbol Pin No in ( )	0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Test Conditions Vdc ±1% @ Test Temperature 0°C	—	−0.850	−1.350	−5.20	−1.18										
+25°C	−0.670	−0.795	−1.350	−5.20	−1.15										
+75°C	—	−0.725	−1.350	−5.20	−1.08										
Power Supply Drain Current	—	—	—	2,6,7,0	1	4,5	3	I_E (2)	—	68	—	65	—	63	mAdc
Input Current	6	—	—	2,7,0	1	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8	1	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	0	—	—	2,6,7	1	—	3	I_{in} (8)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	2,7,0	1	4,5	3	V_1 (6)	−0.695	−0.850	−0.650	−0.795	−0.570	−0.725	Vdc
	—	—	7	2,6,0	1	4,5	3	V_1 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	4,5	3	V_1 (8)							
"NOR" Logical "0" Output Voltage	—	6	—	2,7,0	1	4,5	3	V_4 (6)	−1.495	−1.000	−1.450	−1.750	−1.395	−1.730	Vdc
	—	7	—	2,6,0	1	4,5	3	V_4 (7)	↓	↓	↓	↓	↓	↓	↓
	—	0	—	2,6,7	1	4,5	3	V_4 (8)							
"OR" Logical "1" Output Voltage	—	6	—	2,7,8	1	4,5	3	V_2 (6)	−0.695	−0.050	−0.650	−0.795	−0.570	−0.725	Vdc
	—	7	—	2,6,0	1	4,5	3	V_2 (7)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	4,5	3	V_2 (8)							
"OR" Logical "0" Output Voltage	—	—	6	2,7,0	1	4,5	3	V_5 (6)	−1.495	−1.880	−1.450	−1.750	−1.395	−1.730	Vdc
	—	—	7	2,6,8	1	4,5	3	V_5 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	0	2,6,7	1	4,5	3	V_5 (0)							
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	2,7,8	1	—	3	t_{d1} (5)	12.0	20.0	12.0	20.0	13.5	25.0	ns
	6	4	—	2,7,0	1	—	3	t_{d1} (4)	16.0	25.0	16.0	25.0	18.5	30.0	↓
	6	5	—	2,7,0	1	—	3	t_{d2} (5)	14.0	25.0	14.0	25.0	16.0	30.0	
	6	4	—	2,7,0	1	—	3	t_{d2} (4)	10.0	20.0	10.0	20.0	11.0	23.0	
Rise Time	6	5	—	2,7,0	1	—	3	t_r (5)	16.5	25.0	16.0	25.0	19.0	30.0	
	6	4	—	2,7,0	1	—	3	t_r (4)	13.0	20.0	13.0	20.0	15.5	25.0	
Fall Time	6	5	—	2,7,0	1	—	3	t_f (5)	20.5	35.0	20.5	35.0	26.0	47.0	
	6	4	—	2,7,0	1	—	3	t_f (4)	20.0	35.0	20.0	35.0	23.0	47.0	

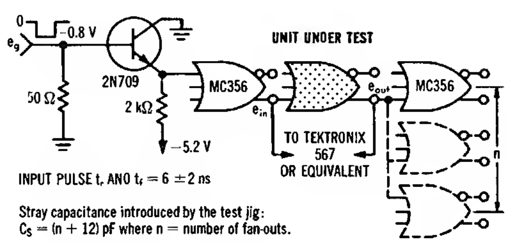
Pins not listed are left open. ① Output is loaded with a 50-ohm resistor.

MC369G

High-speed clock driver or dual 2-input gate that provides the positive logic "NOR" function and its complement simultaneously.



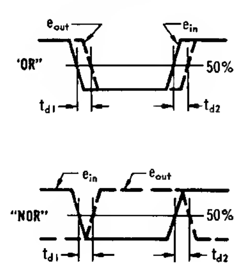
SWITCHING TIME TEST CIRCUIT



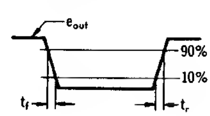
INPUT PULSE t_r AND $t_f = 6 \pm 2$ ns

Stray capacitance introduced by the test jig:
$C_S = (n + 12)$ pF where n = number of fan-outs.

PROPAGATION DELAY



RISE AND FALL TIME



ELECTRICAL CHARACTERISTICS

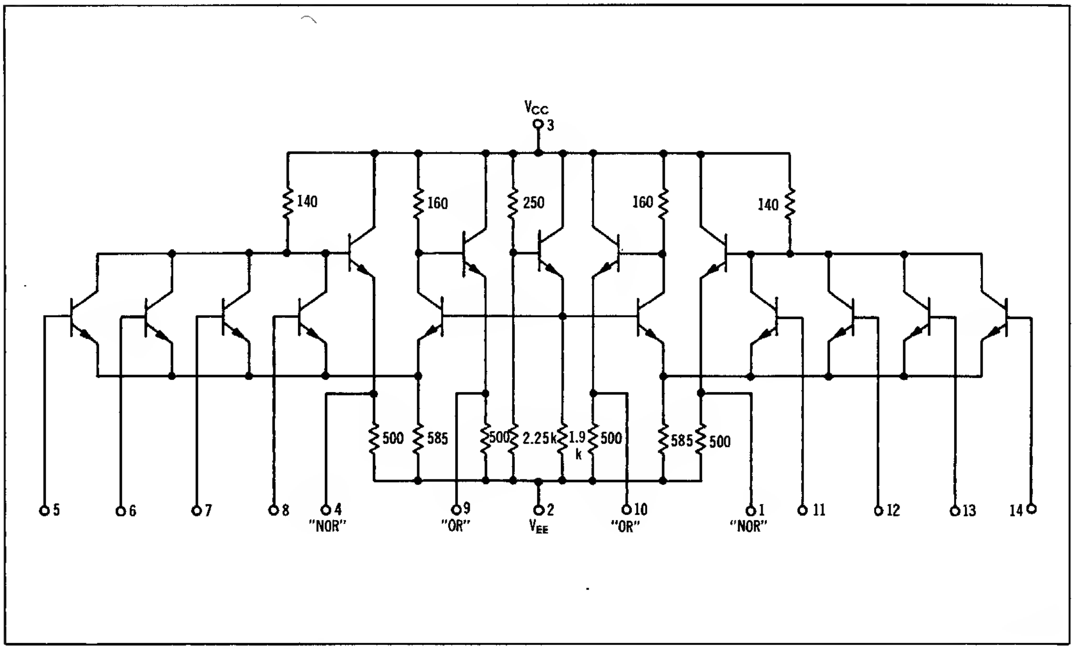
@ Test Temperature	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.510	−5.20
+25°C	−0.670	−0.795	−1.465	−5.20
+75°C	—	−0.725	−1.395	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Oraln Current	—	—	—	2,5,6,9,10	—	—	3	I_E (2)	—	—	—	60	—	—	mAdc
Input Current	5	—	—	2,6,9,10	—	—	3	I_{in} (5)	—	—	—	200	—	—	μAdc
	6	—	—	2,5,9,10	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	9	—	—	2,5,6,10	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	2,5,6,9	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	5	2,6,9,10	—	—	3	V_1 (4)	−0.700	−0.900	−0.650	−0.625	−0.550	−0.770	Vdc
	—	—	6	2,5,9,10	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,5,6,10	—	—	3	V_1 (1)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	2,5,8,9	—	—	3	V_1 (1)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "6" Output Voltage	—	5	—	2,6,9,10	—	—	3	V_4 (4)	−1.510	−1.680	−1.465	−1.650	−1.395	−1.790	Vdc
	—	6	—	2,5,9,10	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,5,6,10	—	—	3	V_4 (1)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	2,5,6,9	—	—	3	V_4 (1)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "1" Output Voltage	—	5	—	2,6,9,10	—	—	3	V_5 (7)	−0.700	−0.900	−0.650	−0.825	−0.550	−0.770	Vdc
	—	6	—	2,5,9,10	—	—	3	V_5 (7)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,5,6,10	—	—	3	V_5 (6)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	2,5,8,9	—	—	3	V_5 (8)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "0" Outpet Voltage	—	—	5	2,6,9,10	—	—	3	V_2 (7)	−1.510	−1.880	−1.465	−1.650	−1.395	−1.790	Vdc
	—	—	6	2,5,9,10	—	—	3	V_2 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,5,6,10	—	—	3	V_2 (6)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	2,5,6,9	—	—	3	V_2 (8)	↓	↓	↓	↓	↓	↓	↓
"NOR" Outpet Voltage Change	—	—	5	2,6,9,10	—	4②	3	ΔV_1 (4)	—	−0.100	—	−0.100	—	−0.130	Volts
	—	—	9	2,5,6,10	—	1②	3	ΔV_1 (1)	—	−0.100	—	−0.100	—	−0.130	Volts
"OR" 6utput Voltage Change	—	5	—	2,6,9,10	—	7②	3	ΔV_5 (7)	—	−0.100	—	−0.100	—	−0.130	Volts
	—	9	—	2,5,6,10	—	8②	3	ΔV_5 (6)	—	−0.100	—	−0.100	—	−0.130	Voite
"NOR" Saturation Breakpelnt Voltage	—	—	—	2,6,9,10	5①	—	3	V_3 (4)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	2,5,9,10	6①	—	3	V_3 (4)	—	↓	—	↓	—	↓	↓
	—	—	—	2,5,6,10	9①	—	3	V_3 (1)	—	↓	—	↓	—	↓	↓
	—	—	—	2,5,6,9	10①	—	3	V_3 (1)	—	↓	—	↓	—	↓	↓
Switching Timee Propagation Oelay Time	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Fan-Out = 1	5	4	—	2,6,9,10	—	—	3	t_{d1} (4)	3	5	3	5	4	6	ns
	5	7	—	2,6,9,10	—	—	3	t_{d1} (7)	↓	6	↓	6	↓	7	↓
	9	1	—	2,5,6,10	—	—	3	t_{d1} (1)	↓	5	↓	5	↓	6	↓
	9	6	—	2,5,6,10	—	—	3	t_{d1} (6)	↓	6	↓	6	↓	7	↓
	5	4	—	2,6,9,10	—	—	3	t_{d2} (4)	3	6	3	6	4	7	↓
	5	7	—	2,6,9,10	—	—	3	t_{d2} (7)	↓	5	↓	5	↓	6	↓
	9	1	—	2,5,6,10	—	—	3	t_{d2} (1)	↓	6	↓	6	↓	7	↓
	9	8	—	2,5,6,10	—	—	3	t_{d2} (6)	↓	5	↓	5	↓	6	↓
Fan-Out = 10	5	4	—	2,6,9,10	—	—	3	t_{d1} (4)	4	7	4	7	5	6	↓
	5	7	—	2,6,9,10	—	—	3	t_{d1} (7)	5	10	5	10	6	11	↓
	9	1	—	2,5,6,10	—	—	3	t_{d1} (1)	4	7	4	7	5	6	↓
	9	6	—	2,5,6,10	—	—	3	t_{d1} (8)	5	10	5	10	6	11	↓
	5	4	—	2,6,9,10	—	—	3	t_{d2} (4)	5	10	5	10	6	11	↓
	5	7	—	2,6,9,10	—	—	3	t_{d2} (7)	4	7	4	7	5	6	↓
	9	1	—	2,5,6,10	—	—	3	t_{d2} (1)	5	10	5	10	6	11	↓
	9	6	—	2,5,6,10	—	—	3	t_{d2} (8)	4	7	4	7	5	6	↓
Rise Time, Fan-Out = 1	5	4	—	2,6,9,10	—	—	3	t_r (4)	4	7	4	7	5	9	↓
	5	7	—	2,6,9,10	—	—	3	t_r (7)	↓	6	↓	6	↓	6	↓
	9	1	—	2,5,6,10	—	—	3	t_r (1)	↓	7	↓	7	↓	9	↓
	9	6	—	2,5,6,10	—	—	3	t_r (6)	↓	6	↓	6	↓	6	↓
Fan-Out = 10	5	4	—	2,6,9,10	—	—	3	t_r (4)	4	9	4	9	5	10	↓
	5	7	—	2,6,9,10	—	—	3	t_r (7)	↓	↓	↓	↓	↓	↓	↓
	9	1	—	2,5,6,10	—	—	3	t_r (1)	↓	↓	↓	↓	↓	↓	↓
	9	6	—	2,5,6,10	—	—	3	t_r (6)	↓	↓	↓	↓	↓	↓	↓
Fall Time, Fan-Out = 1	5	4	—	2,6,9,10	—	—	3	t_f (4)	4	6	4	6	5	7	↓
	5	7	—	2,6,9,10	—	—	3	t_f (7)	↓	↓	↓	↓	↓	↓	↓
	9	1	—	2,5,6,10	—	—	3	t_f (1)	↓	↓	↓	↓	↓	↓	↓
	9	6	—	2,5,6,10	—	—	3	t_f (8)	↓	↓	↓	↓	↓	↓	↓
Fan-Out = 10	5	4	—	2,6,9,10	—	—	3	t_f (4)	6	11	6	11	7	12	↓
	5	7	—	2,6,9,10	—	—	3	t_f (7)	↓	↓	↓	↓	↓	↓	↓
	9	1	—	2,5,6,10	—	—	3	t_f (1)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	2,5,6,10	—	—	3	t_f (6)	↓	↓	↓	↓	↓	↓	↓

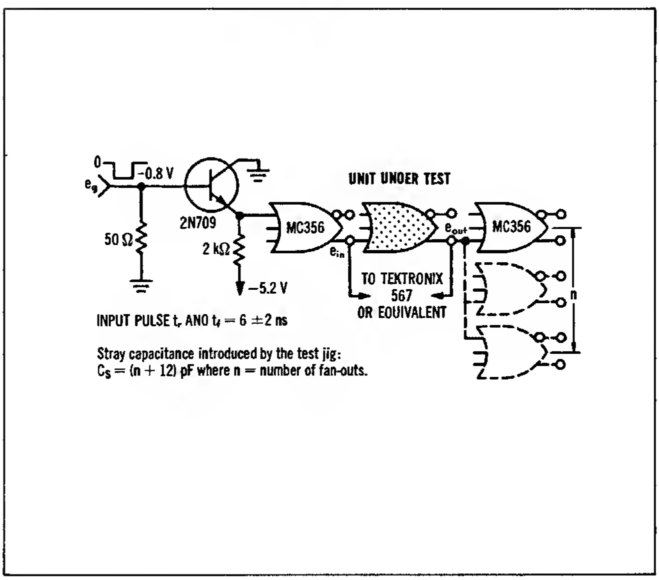
Pins not listed are left open. ① Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0. ② Current test conditions: no load = 0; full load = −10 mAdc ±5%.

MC369F

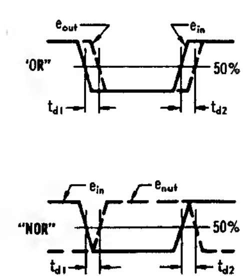
High-speed clock driver or dual 4-input gate that provides the positive logic "NOR" function and its complement simultaneously.



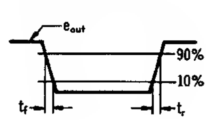
SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY



RISE AND FALL TIME



ELECTRICAL CHARACTERISTICS

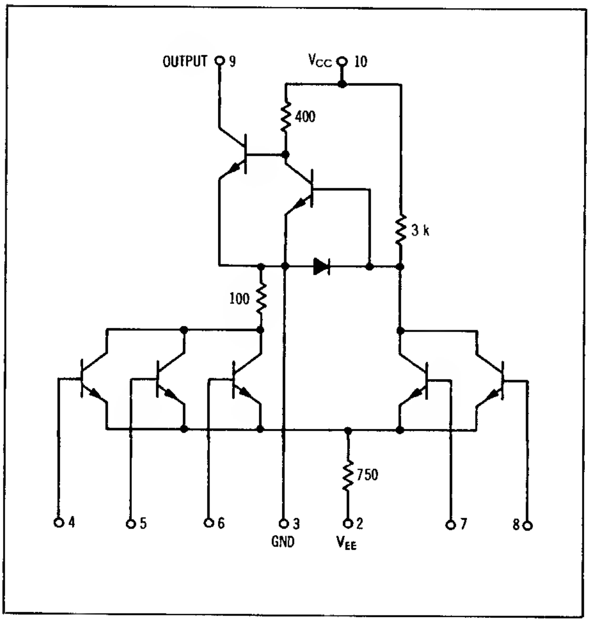
@ Test Temperature	V_H	$V_{I\,max}$	V_L	V_{EE}
	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.510	−5.20
+25°C	−0.670	−0.795	−1.465	−5.20
+75°C	—	−0.725	−1.395	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,5,6,7,8,11,12,13,14	—	—	3	I_E (2)	—	—	—	60	—	—	mAdc
Input Current	5	—	—	2,6,7,8,11,12,13,14	—	—	3	I_{in} (5)	—	—	—	200	—	—	µAdc
	6	—	—	2,5,7,8,11,12,13,14	—	—	3	I_{in} (6)	—	—	—		—	—	
	7	—	—	2,5,6,8,11,12,13,14	—	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	2,5,6,7,11,12,13,14	—	—	3	I_{in} (8)	—	—	—		—	—	
	11	—	—	2,5,6,7,8,12,13,14	—	—	3	I_{in} (11)	—	—	—		—	—	
	12	—	—	2,5,6,7,8,11,13,14	—	—	3	I_{in} (12)	—	—	—		—	—	
	13	—	—	2,5,6,7,8,11,12,14	—	—	3	I_{in} (13)	—	—	—		—	—	
	14	—	—	2,5,6,7,8,11,12,13	—	—	3	I_{in} (14)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	5	2,6,7,8,11,12,13,14	—	—	3	V_1 (4)	−0.700	−0.900	−0.650	−0.825	−0.550	−0.770	Vdc
	—	—	6	2,5,7,8,11,12,13,14	—	—	3	V_1 (4)							
	—	—	7	2,5,6,8,11,12,13,14	—	—	3	V_1 (4)							
	—	—	8	2,5,8,7,11,12,13,14	—	—	3	V_1 (4)							
	—	—	11	2,5,6,7,8,12,13,14	—	—	3	V_1 (1)							
	—	—	12	2,5,6,7,8,11,13,14	—	—	3	V_1 (1)							
	—	—	13	2,5,6,7,8,11,12,14	—	—	3	V_1 (1)							
	—	—	14	2,5,6,7,8,11,12,13	—	—	3	V_1 (1)							
"NOR" Logical "0" Output Voltage	—	5	—	2,6,7,8,11,12,13,14	—	—	3	V_4 (4)	−1.510	−1.880	−1.465	−1.850	−1.395	−1.790	Vdc
	—	6	—	2,5,7,8,11,12,13,14	—	—	3	V_4 (4)							
	—	7	—	2,5,6,8,11,12,13,14	—	—	3	V_4 (4)							
	—	8	—	2,5,6,7,11,12,13,14	—	—	3	V_4 (4)							
	—	11	—	2,5,6,7,8,12,13,14	—	—	3	V_4 (1)							
	—	12	—	2,5,6,7,8,11,13,14	—	—	3	V_4 (1)							
	—	13	—	2,5,6,7,8,11,12,14	—	—	3	V_4 (1)							
	—	14	—	2,5,6,7,8,11,12,13	—	—	3	V_4 (1)							
"OR" Logical "1" Output Voltage	—	5	—	2,6,7,8,11,12,13,14	—	—	3	V_5 (9)	−0.700	−0.900	−0.650	−0.825	−0.550	−0.770	Vdc
	—	6	—	2,5,7,8,11,12,13,14	—	—	3	V_5 (9)							
	—	7	—	2,5,6,8,11,12,13,14	—	—	3	V_5 (9)							
	—	8	—	2,5,6,7,11,12,13,14	—	—	3	V_5 (9)							
	—	11	—	2,5,6,7,8,12,13,14	—	—	3	V_5 (10)							
	—	12	—	2,5,6,7,8,11,13,14	—	—	3	V_5 (10)							
	—	13	—	2,5,6,7,8,11,12,14	—	—	3	V_5 (10)							
	—	14	—	2,5,6,7,8,11,12,13	—	—	3	V_5 (10)							
"OR" Logical "0" Output Voltage	—	—	5	2,6,7,8,11,12,13,14	—	—	3	V_2 (9)	−1.510	−1.880	−1.465	−1.850	−1.395	−1.790	Vdc
	—	—	8	2,5,7,8,11,12,13,14	—	—	3	V_2 (9)							
	—	—	7	2,5,6,8,11,12,13,14	—	—	3	V_2 (9)							
	—	—	8	2,5,6,7,11,12,13,14	—	—	3	V_2 (9)							
	—	—	11	2,5,6,7,8,12,13,14	—	—	3	V_2 (10)							
	—	—	12	2,5,6,7,8,11,13,14	—	—	3	V_2 (10)							
	—	—	13	2,5,6,7,8,11,12,14	—	—	3	V_2 (10)							
	—	—	14	2,5,6,7,8,11,12,13	—	—	3	V_2 (10)							
"NOR" Output Voltage Change	—	—	5	2,6,7,8,11,12,13,14	—	4②	3	ΔV_1 (4)	—	−0.100	—	−0.100	—	−0.130	Volts
	—	—	11	2,5,6,7,8,12,13,14	—	1②	3	ΔV_1 (1)	—	−0.100	—	−0.100	—	−0.130	Volts
"OR" Output Voltage Change	—	5	—	2,6,7,8,11,12,13,14	—	9②	3	ΔV_5 (9)	—	−0.100	—	−0.100	—	−0.130	Volts
	—	11	—	2,5,6,7,8,12,13,14	—	10②	3	ΔV_5 (10)	—	−0.100	—	−0.100	—	−0.130	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,11,12,13,14	5①	—	3	V_3 (5)	—	−0.51	—	−0.55	—	−0.83	Vdc
	—	—	—	2 5,7,8,11,12,13,14	8①	—	3	V_3 (6)	—		—		—		
	—	—	—	2 5,6,8,11,12,13,14	7①	—	3	V_3 (7)	—		—		—		
	—	—	—	2,5,6,7,11,12,13,14	8①	—	3	V_3 (8)	—		—		—		
	—	—	—	2,5,6,7,8,12,13,14	11①	—	3	V_3 (11)	—		—		—		
	—	—	—	2,5,6,7,8,11,13,14	12①	—	3	V_3 (12)	—		—		—		
	—	—	—	2,5,6,7,8,11,12,14	13①	—	3	V_3 (13)	—		—		—		
	—	—	—	2,5,6,7,8,11,12,13	14①	—	3	V_3 (14)	—		—		—		
Switching Times Propagation Delay Time	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Fan-Out = 1	5	4	—	2 6,7,8,11,12,13,14	—	—	3	t_{d1} (4)	3	5	3	5	4	6	ns
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_{d1} (9)		8		6		7	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_{d1} (1)		5		5		6	
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_{d1} (10)		6		6		7	
	5	4	—	2 6,7,8,11,12,13,14	—	—	3	t_{d2} (4)	3	6	3	6	4	7	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_{d2} (9)		5		5		6	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_{d2} (1)		6		8		7	
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_{d2} (10)		5		5		6	
Fan-Out = 10	5	4	—	2 6,7,8,11,12,13,14	—	—	3	t_{d1} (4)	4	7	4	7	5	8	
	5	9	—	2 6,7,8,11,12,13,14	—	—	3	t_{d1} (9)	5	10	5	10	6	11	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_{d1} (1)	4	7	4	7	5	8	
	11	10	—	2,5,6 7,8,12,13,14	—	—	3	t_{d1} (10)	5	10	5	10	6	11	
	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_{d2} (4)	5	10	5	10	6	11	
	5	9	—	2 6,7,8,11,12,13,14	—	—	3	t_{d2} (9)	4	7	4	7	5	8	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_{d2} (1)	5	10	5	10	6	11	
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_{d2} (10)	4	7	4	7	5	8	
Rise Time, Fan-Out = 1	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_r (4)	4	7	4	7	5	9	
	5	9	—	2 6,7,8,11,12,13,14	—	—	3	t_r (9)		8		8		8	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_r (1)		7		7		9	
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_r (10)		8		6		8	
Fan-Out = 10	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_r (4)	4	9	4	9	5	10	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_r (9)							
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_r (1)							
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_r (10)							
Fall Time, Fan-Out = 1	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_f (4)	4	6	4	6	5	7	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_f (9)							
	11	1	—	2,5,6.7,8,12,13,14	—	—	3	t_f (1)							
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_f (10)							
Fan-Out = 10	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_f (4)	6	11	8	11	7	12	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_f (9)							
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_f (1)							
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_f (10)							

Pins not listed are left open. ① Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0. ② Current test conditions: no load = 0; full load = −10 mAdc ±5%.

MC366

Lamp driver that provides "OR" or "NOR" logic depending on the bias arrangement used and is capable of driving 6V lamps.



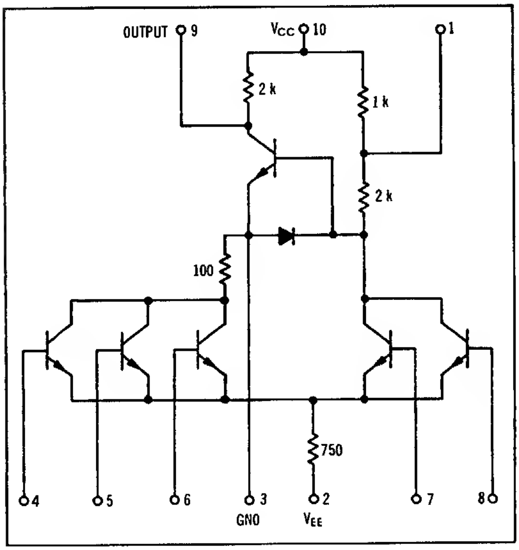
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%						mAdc									
0°C	—	−0.850	−1.350	−5.20	−1.18	+6.0	100									
+25°C	−0.670	−0.795	−1.350	−5.20	−1.15	+6.0	100									
+75°C	—	−0.725	−1.350	−5.20	−1.08	+6.0	100									
										Test Limits						
										0°C		+25°C		+75°C		
Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	—	4,5,6	—	2,7	8	10	—	3	I_C (10)	—	22.5	—	21.5	—	20.7	mAdc
	—	4,5,6	—	2,7	8	10	—	3	I_E (2)	—	8.4	—	8.0	—	7.7	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	μAdc
	5	—	—	2,4,6,7	8	10	—	3	I_{in} (5)	—	—	—	↓	—	—	↓
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	2,4,5,6	8	10	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,4,5,7	6	10	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
Output Voltage, Low	—	—	6	2,4,5,7	8	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	1.25	Vdc
	—	—	6	2,4,5,8	7	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	1.25	Vdc
Output Voltage, High	—	4	—	2,5,6,7	8	10,9①	—	3	V_{OH} (4)	—	—	—	5.8	—	5.8	Vdc
	—	5	—	2,4,6,7	8	10,9①	—	3	V_{OH} (5)	—	—	—	↓	—	↓	↓
	—	6	—	2,4,5,7	8	10,9①	—	3	V_{OH} (6)	—	—	—	↓	—	↓	↓
	—	6	—	2,4,5,8	7	10,9①	—	3	V_{OH} (6)	—	—	—	↓	—	↓	↓

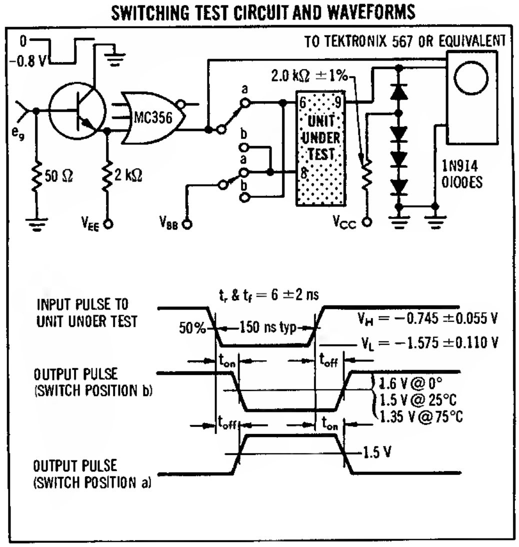
Pins not listed are left open. ① Pin 9 is connected to Vcc through a 10 k-ohm resistor.

MC367

Level translator intended for converting non-saturated MECL signal levels to saturated logic levels; provides "OR" or "NOR" logic depending on the bias arrangement used.



SWITCHING TEST CIRCUIT AND WAVEFORMS

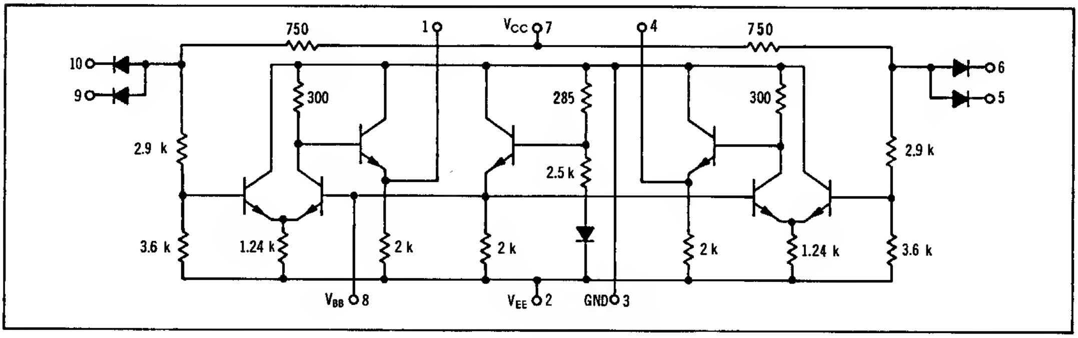


ELECTRICAL CHARACTERISTICS

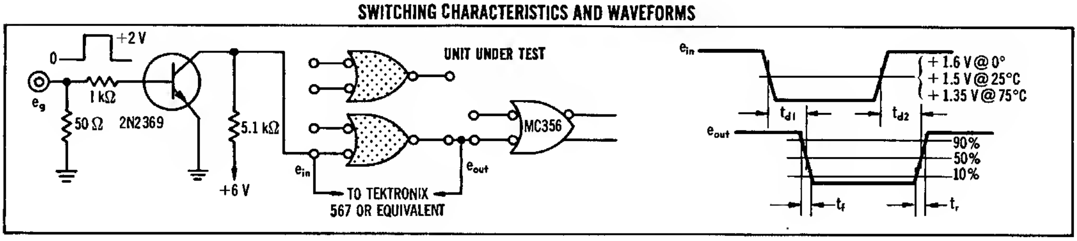
	Test Conditions Vdc ±1%						mAdc									
@ Test Temperature 0°C	—	−0.850	−1.350	−5.20	−1.18	+6.0	10									
@ Test Temperature +25°C	−0.670	−0.795	−1.350	−5.20	−1.15	+6.0	10									
@ Test Temperature +75°C	—	−0.725	−1.350	−5.20	−1.08	+6.0	10							Test Limits		
										0°C		+25°C		+75°C		
Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	—	6	—	2,4,5,7	6	10	—	3	I_C (10)	—	7.3	—	7.0	—	6.6	mAdc
	—	—	—	2,4,5,6,7	8	10	—	3	I_E (2)	—	7.3	—	7.0	—	6.8	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	µAdc
	5	—	—	2,4,6,7	8	10	—	3	I_{in} (5)	—	—	—	↓	—	—	↓
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	2,4,5,6	6	10	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,4,5,7	6	10	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
Output Voltage, High	—	—	—	2,4,5,6,7	8	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
	—	—	—	2,4,5,6,8	7	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
Output Voltage, Low	—	4	—	2,5,6,7	8	10	9	3	V_{OL} (9)	—	0.45	—	0.45	—	0.50	Vdc
	—	5	—	2,4,6,7	8	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
	—	6	—	2,4,5,7	8	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
	—	6	—	2,4,5,6	7	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Turn-On Time	6	9	—	2,4,5,7	6	10	—	3	t_{on} (9)	27.5	40.0	27.5	40.0	29.5	43.0	ns
	6	9	—	2,4,5,7	6	10	—	3	t_{on} (9)	27.5	40.0	27.5	40.0	29.5	43.0	↓
Turn-Off Time	6	9	—	2,4,5,7	8	10	—	3	t_{off} (9)	25.0	40.0	26.0	40.0	27.0	43.0	↓
	6	9	—	2,4,5,7	6	10	—	3	t_{off} (9)	25.0	40.0	26.0	40.0	27.0	43.0	↓

MC368

Level translator intended for converting saturated logic levels to non-saturated MECL signal levels.



SWITCHING CHARACTERISTICS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
0°C	+0.45	+5.0	−5.20	+6.0
+25°C	+0.45	+5.0	−5.20	+6.0
+75°C	+0.50	+5.0	−5.20	+6.0

Characteristic	V_{IL} Pin No	V_{IH} Pin No	V_{EE} Pin No	V_{CC} Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	2	7	3	I_C (7)	—	4.2	—	4.0	—	3.9	mAdc
	—	—	2	7	3	I_E (2)	—	21.9	—	21.0	—	20.2	mAdc
Input Load Current	—	—	2	7	3,5	I_L (5)	—	—	—	8.5	—	—	mAdc
	—	—	2	7	3,6	I_L (6)	—	—	—	↓	—	—	↓
	—	—	2	7	3,9	I_L (9)	—	—	—	↓	—	—	↓
	—	—	2	7	3,10	I_L (10)	—	—	—	↓	—	—	↓
Input Reverse Current	—	—	2	5,7	3,6	I_R (5)	—	—	—	0.5	—	2.0	μAdc
	—	—	2	6,7	3,5	I_R (6)	—	—	—	↓	—	↓	↓
	—	—	2	7,9	3,10	I_R (9)	—	—	—	↓	—	↓	↓
	—	—	2	7,10	3,9	I_R (10)	—	—	—	↓	—	↓	↓
"OR" Logical "1" Output Voltage	—	5	2	7	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.570	−0.725	Vdc
	—	6	2	7	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	2	7	3	V_5 (1)	↓	↓	↓	↓	↓	↓	↓
	—	10	2	7	3	V_5 (1)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "0" Output Voltage	5	—	2	7	3	V_2 (4)	−1.510	−1.880	−1.450	−1.750	−1.395	−1.730	Vdc
	6	—	2	7	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	9	—	2	7	3	V_2 (1)	↓	↓	↓	↓	↓	↓	↓
	10	—	2	7	3	V_2 (1)	↓	↓	↓	↓	↓	↓	↓
Bias Voltage Output	—	—	2	7	3	V_{BB} (8)	−1.14	−1.27	−1.09	−1.22	−1.04	−1.18	Vdc
Switching Times	Pulse In	Pulse Out					Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	5	4	2	7	3	t_{d1} (4)	14.5	24.0	15.0	24.0	19.0	28.0	ns
	9	1	2	7	3	t_{d1} (1)	14.5	24.0	15.0	24.0	19.0	28.0	↓
	5	4	2	7	3	t_{d2} (4)	15.5	23.0	15.5	23.0	19.0	28.0	↓
	9	1	2	7	3	t_{d2} (1)	15.5	23.0	15.5	23.0	19.0	28.0	↓
Rise Time	5	4	2	7	3	t_r (4)	6.5	13.0	7.0	13.0	8.0	14.0	↓
	9	1	2	7	3	t_r (1)	6.5	13.0	7.0	13.0	8.0	14.0	↓
Fall Time	5	4	2	7	3	t_f (4)	7.0	13.0	7.5	13.0	8.0	14.0	↓
	9	1	2	7	3	t_f (1)	7.0	13.0	7.5	13.0	8.0	14.0	↓

Pins not listed are left open.

MECL II

INTEGRATED CIRCUITS
MC1000/MC1200 SERIES

MECL II

INTEGRATED CIRCUITS

INDEX

NUMERICAL INDEX
(Functions and Characteristics)

$V_{CC} = 0$, $V_{EE} = -5.2$ V, $T_A = 25^oC$

Function	Type: Case 83 −55 to +125°C	Type: Case 93 0 to +75°C	DC Output Loading Factor each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ	Page No.
Single 6-Input Gate, 3 "OR" Outputs w Pulldowns 3 "NOR" Outputs w Pulldowns	MC1201F	MC1001P	25	4.0	115	2–89
Single 6-Input Gate, 3 "OR" Outputs w Pulldowns 3 "NOR" Outputs w/o Pulldowns	MC1202F	MC1002P			80	
Single 6-Input Gate, 3 "OR" Outputs w/o Pulldowns 3 "NOR" Outputs w/o Pulldowns	MC1203F	MC1003P			40	
Dual 4-Input Gate, 2 "OR" Outputs w Pulldowns 2 "NOR" Outputs w Pulldowns	MC1204F	MC1004P			95	2–99
Dual 4-Input Gate, 2 "OR" Outputs w Pulldowns 2 "NOR" Outputs w/o Pulldowns	MC1205F	MC1005P			65	
Dual 4-Input Gate, 2 "OR" Outputs w/o Pulldowns 2 "NOR" Outputs w/o Pulldowns	MC1206F	MC1006P			45	
Triple 3-Input Gate, 3 "NOR" Outputs w Pulldowns	MC1207F	MC1007P			110	2–103
Triple 3-Input Gate, {1 "NOR" Output w Pulldowns {2 "NOR" Outputs w/o Pulldowns	MC1208F	MC1008P			75	
Triple 3-Input Gate, 3 "NOR" Outputs w/o Pulldowns	MC1209F	MC1009P			60	
Quad 2-Input Gate, 4 "NOR" Outputs w Pulldowns	MC1210F	MC1010P			115	2–107
Quad 2-Input Gate, {2 "NOR" Output w Pulldowns {2 "NOR" Output w/o Pulldowns	MC1211F	MC1011P			95	
Quad 2-Input Gate, 4 "NOR" Outputs w/o Pulldowns	MC1212F	MC1012P			65	
85 MHz AC Coupled J-K Flip-Flop	MC1213F	MC1013P		6.0	125	2–119
Dual R-S Flip-Flop (Positive Clock)	MC1214F	MC1014P			140	2–133
Dual R-S Flip-Flop (Negative Clock)	MC1215F	MC1015P			140	2–137
Dual R-S Flip-Flop (Single Rail, Positive Clock)	MC1216F	MC1016P			140	2–141
Level Translator (Sat. Logic to MECL)	MC1217F	MC1017P	25 (MECL)	15	105	2–157
Level Translator (MECL to Sat. Logic)	MC1218F	MC1018P	7 (DTL)	20	70	2–161
Full Adder	MC1219F	MC1019P	25	4.0	110	2–173
Quad Line Receiver	MC1220F	MC1020P			115	2–165
Full Subtractor	MC1221F	MC1021P			110	2–177
Type "D" Flip-Flops	MC1222F	MC1022P		8.0	110	2–153
Dual 4-Input "OR/NOR" Clock Driver	–	MC1023P		2.0	250	2–185
Dual 2-Input Expandable Gate	MC1224F	MC1024P		4.0	95	2–93
Dual 4 and 5 Input Expander	MC1225F	MC1025P	–	–	–	2–97
120 MHz AC Coupled J-K Flip-Flop	–	MC1027P	25	4.0	250	2–127
Data Distributor	MC1229F	MC1029P		4.0	160	2–181
Quad Exclusive OR Gate	MC1230F	MC1030P		5.0	130	2–111
Quad Exclusive NOR Gate	MC1231F	MC1031P		5.0	130	2–115
Dual R-S Flip-Flop (Single Rail, Negative Clock)	MC1233F	MC1033P		6.0	140	2–147
16-Bit Coincident Memory	–	MC1036P	5	17	250	2–169
16-Bit Coincident Memory w/o Pulldowns	–	MC1037P	5	17	250	2–169

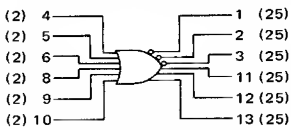
The logic diagrams shown describe the circuits of the MECL II line and permit quick selection of those circuits required to implement a particular logic system. Pertinent information, such as logic equations, truth tables, typical propagation delay time (t_{pd}), and typical power dissipation per package (P_D) is provided to show line compatibility. Package pin numbers and dc loading factors for each device are specified on each logic diagram. The numbers at the ends of the terminals are package pin numbers. The numbers in parentheses indicate dc loading factors at each terminal.

MECL II circuits contain internal bias networks, insuring that the transistion point is always in the center of the transfer characteristic curves over the temerature range.

(V_{CC} = PIN 14, V_{EE} = PIN 7)

GATES

MC1001P, MC1002P, MC1003P MC1201F, MC1202F, MC1203F
6-Input Gate



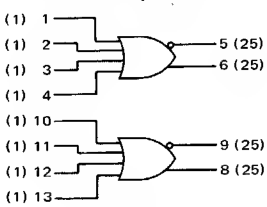
$1 = \overline{4+5+6+8+9+10}$

$11 = 4+5+6+8+9+10$

t_{pd} = 4.0 ns

P_D = MC1001/MC1201 – 115 mW
MC1002/MC1202 – 80 mW
MC1003/MC1203 – 40 mW

MC1004P, MC1005P, MC1006P MC1204F, MC1205F, MC1206F
Dual 4-Input Gate



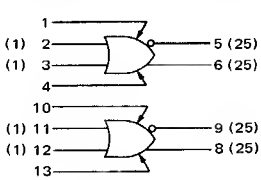
$5 = \overline{1+2+3+4}$

$6 = 1+2+3+4$

t_{pd} = 4.0 ns

P_D = MC1004/MC1204 – 95 mW
MC1005/MC1205 – 65 mW
MC1006/MC1206 – 45 mW

MC1024P, MC1224F
Dual 2-Input Expandable Gate



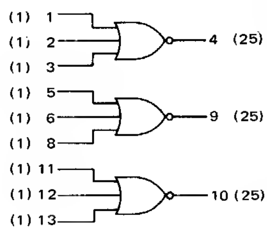
$5 = \overline{2+3}$

$6 = 2+3$

t_{pd} = 4.0 ns

P_D = 95 mW

MC1007P, MC1008P, MC1009P MC1207F, MC1208F, MC1209F
Triple 3-Input Gate

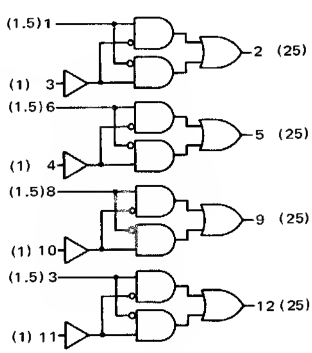


$4 = \overline{1+2+3}$

t_{pd} = 4.0 ns

P_D = MC1007/MC1207 – 110 mW
MC1008/MC1208 – 75 mW
MC1009/MC1209 – 60 mW

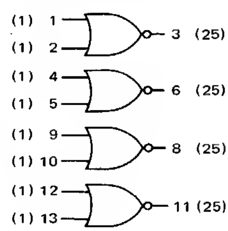
MC1030P, MC1230F
Quad Exclusive OR Gate



$2 = 1 \cdot \overline{3} + \overline{1} \cdot 3$

t_{pd} = 5.0 ns
P_D = 130 mW

MC1010P, MC1011P, MC1012P MC1210F, MC1211F, MC1212F
Quad 2-Input Gate

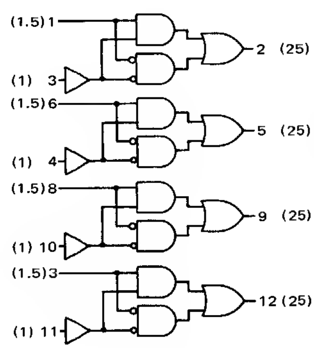


$3 = \overline{1+2}$

t_{pd} = 4.0 ns

P_D = MC1010/MC1210 – 115 mW
MC1011/MC1211 – 95 mW
MC1012/MC1212 – 65 mW

MC1031P, MC1231F
Quad Exclusive NOR Gate

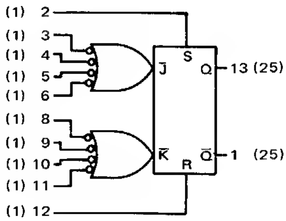


$2 = 1 \cdot 3 + \overline{1} \cdot \overline{3}$

t_{pd} = 5.0 ns
P_D = 130 mW

FLIP-FLOPS

MC1013P, MC1213F
85 MHz AC-Coupled J-K Flip Flop



t_{pd} = 6.0 ns
P_D = 125 mW

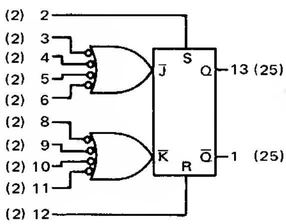
CLOCKED J-K OPERATION

$\bar{J}$	$\bar{K}$	$\bar{C}_D$	Q^n
φ	φ	0	Q^n
0	0	1	$\bar{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n

The $\bar{J}$ and $\bar{K}$ inputs refer to logic level's while the $\bar{C}_D$ input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to a logical "1" only while the $\bar{C}_D$ input is in a logic "1" state. ($\bar{C}_D$ maximum "1" level = V_{CC} − 0.6 V.) Clock $\bar{C}_D$ is obtained by tying one $\bar{J}$ and one $\bar{K}$ input together.

R-S OPERATION

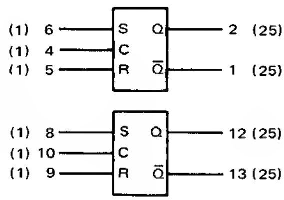
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



t_{pd} = 4.0 ns
P_D = 250 mW

MC1027P
120 MHz AC-Coupled J-K Flip-Flop

MC1014P, MC1214F
MC1015P, MC1215F
Dual Clocked R-S Flip-Flop



t_{pd} = 6.0 ns
P_D = 140 mW

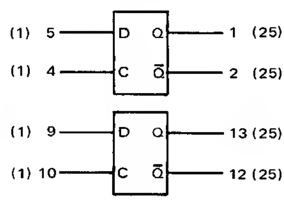
MC1014/1214

C	R	S	Q^{n+1}
1	0	0	Q^n
1	0	1	1
1	1	0	0
1	1	1	ND
0	φ	φ	Q^n

MC1015/1215

C	R	S	Q^{n+1}
0	0	0	Q^n
0	0	1	1
0	1	0	0
0	1	1	ND
1	φ	φ	Q^n

MC1016P, MC1216F
MC1033P, MC1233F
Dual Clocked Single Rail R-S Flip-Flop



t_{pd} = 6.0 ns
P_D = 140 mW

MC1016/1216

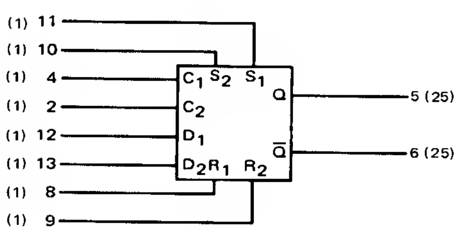
C	D	Q^{n+1}
0	0	Q^n
0	1	Q^n
1	0	0
1	1	1

MC1033/1233

C	D	Q^{n+1}
1	0	Q^n
1	1	Q^n
0	0	0
0	1	1

MC1022P, MC1222F
Type "D" Flip-Flop

POSITIVE LOGIC



t_{pd} = 8.0 ns
P_D = 110 mW

R-S TRUTH TABLE

	R	S	Q^{n+1}	$\bar{Q}^{n+1}$
Pin No.	8 or 9	10 or 11	5	6
	0	0	Q^n	$\bar{Q}^n$
	0	1	1	0
	1	0	0	1
	1	1	N.D.	N.D.

N.D. = Not Defined

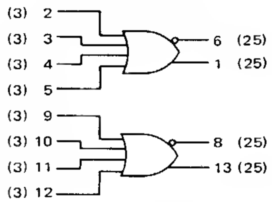
CLOCKED TRUTH TABLE

	D	C	Q^{n+1}	$\bar{Q}^{n+1}$
Pin No.	12 or 13	2 or 4	5	6
	0	0	Q^n	$\bar{Q}^n$
	1	0	Q^n	$\bar{Q}^n$
	0	1*	0	1
	1	1*	1	0

*A "1" or Clock input is defined for this flip-flop as a change in level from a low input to a high input.

DRIVER

MC1023P
Dual 4-Input Clock Driver



$6 = \overline{2+2+4+5}$

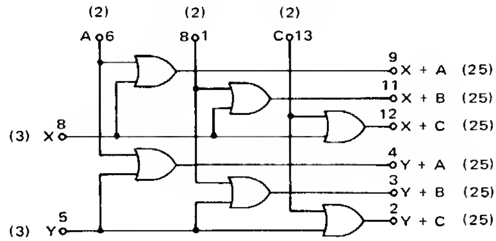
$1 = 2+3+4+5$

$t_{pd} = 2.0$ ns

$P_D = 250$ mW

DATA DISTRIBUTOR

MC1029P, MC1229F
2 X 3 Data Distributor

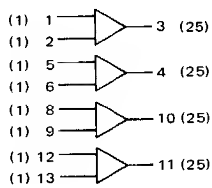


$t_{pd} = 4.0$ ns

$P_D = 160$ mW

RECEIVER

MC1020P, MC1220F
Quad Line Receiver

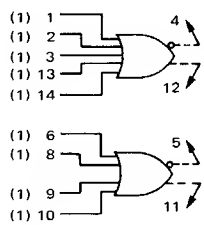


$t_{pd} = 4.0$ ns

$P_D = 115$ mW

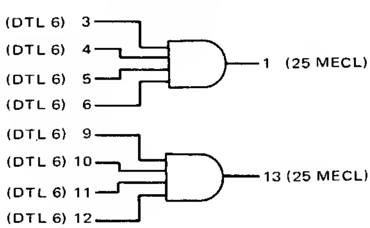
EXPANDER

MC1025P, MC1225F
Dual 4-5 Input Expander



TRANSLATORS

MC1017P, MC1217F
Level Translator

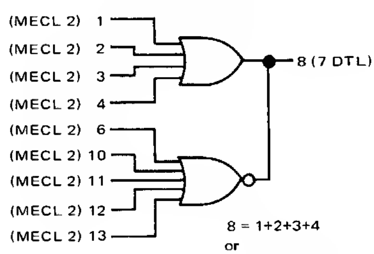


$1 = 3 \bullet 4 \bullet 5 \bullet 6$

$t_{pd} = 15$ ns

$P_D = 105$ mW

MC1018P, MC1218F
Level Translator



$8 = 1+2+3+4$

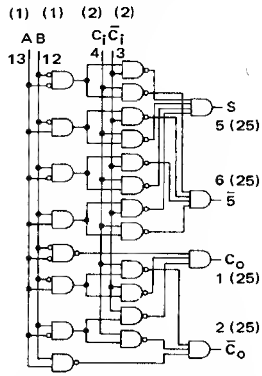
or

$8 = \overline{6+10+11+12+13}$

$t_{pd} = 20$ ns $\quad P_D = 70$ mW

FULL ADDER

MC1019P, MC1219F
Full Adder

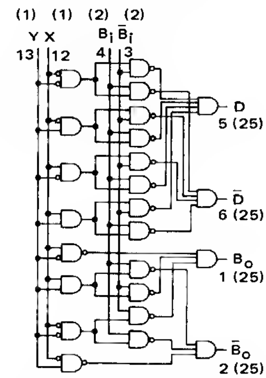


$S = ABC_i + A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i$
$\bar{S} = \bar{A}\bar{B}\bar{C}_i + AB\bar{C}_i + A\bar{B}C_i + \bar{A}BC_i$
$C_o = ABC_i + AB\bar{C}_i + A\bar{B}C_i + \bar{A}BC_i$
$\bar{C}_o = \bar{A}\bar{B}\bar{C}_i + A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i$

$t_{pd} = 4.0$ ns $P_D = 110$ mW

SUBTRACTOR

MC1021P, MC1221F
Full Subtractor

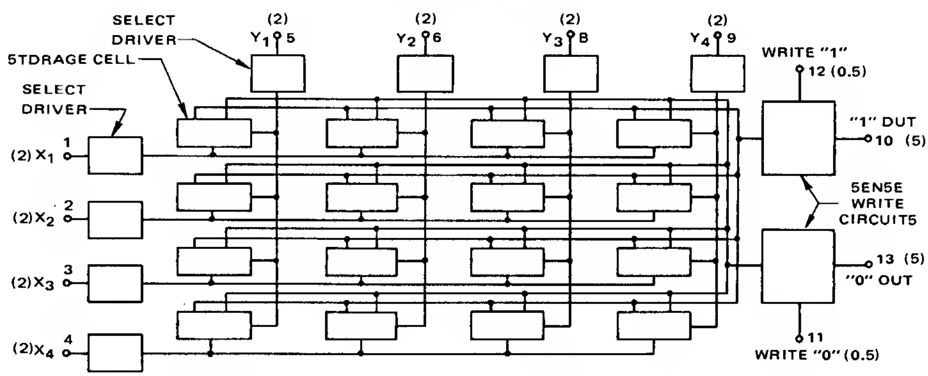


$D = YXB_i + Y\bar{X}\bar{B}_i + \bar{Y}X\bar{B}_i + \bar{Y}\bar{X}B_i$
$\bar{D} = \bar{Y}\bar{X}\bar{B}_i + YX\bar{B}_i + Y\bar{X}B_i + \bar{Y}XB_i$
$B_o = \bar{Y}\bar{X}B_i + Y\bar{X}\bar{B}_i + Y\bar{X}B_i + YXB_i$
$\bar{B}_o = \bar{Y}\bar{X}\bar{B}_i + \bar{Y}X\bar{B}_i + \bar{Y}XB_i + YX\bar{B}_i$

$t_{pd} = 4.0$ ns $P_D = 110$ mW

MEMORY

MC1036P, MC1037P
16-Bit Coincident Memory



$t_{pd} = 17$ ns
$P_D = 250$ mW

Maximum Power Supply Variation = ±10%

MECL II

GENERAL INFORMATION SECTION

INTRODUCTION

The MECL II family of Emitter-coupled Logic (current mode logic) was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic, and permits extremely high-speed operation.

The typical MECL II circuit comprises a differential-amplifier input with internal bias reference and with emitter-follower outputs to restore dc levels. High fan-out operation is possible because of the high input impedance of the differential amplifiers and the low output impedance of the emitter followers. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the function and its complement.

MECL II devices are specified over two temperature ranges: 0 to 75°C (MC1000 Series) and −55 to 125°C (MC1200 Series). The MC1000 Series is available in the dual in-line plastic package (add suffix "P" to basic type number) and the MC1200 Series in the TO-86 ceramic flat package (suffix "F").

Family characteristics are:

- 4.0 ns propagation delay
- DC fan-out of 25 minimum
- High-frequency operation, if required
- Excellent speed-power product
- Constant current drain regardless of logic state or operating frequency
- ±20% power supply tolerance

System features include:

- Minimized cross-talk
- Reduced power dissipation and can count through Wired-OR and the series gating design techniques
- Guaranteed worst-case noise margin
- Single power supply
- Ease of designing parallel rather than serial logic

MECL II DESIGN PHILOSOPHY

The following goals have been met by MECL II, resulting in the most economical form of logic for system design:

I. Availability has been maximized through:
   - A. Non-stringent processing requirements
   - B. Optimized chip and device size
   - C. Specifications determined by distribution data, on parts produced in volume, analyzed for system design requirements.
   - D. Internal specification guard-bands set to minimize correlation problems.

II. Rise and fall times of basic family are kept slow enough to be compatible with conventional layout techniques such as two-sided printed circuit boards and point-to-point backplane wiring.

III. MECL II is compatible with the original MECL (MC300 and MC350 Series).

IV. Logic has been maximized for 14-pin packages by using complex functions wherever economical.

During design, the cost to run a problem or to do a specified amount of work on a system should be considered. To run a problem on a system, the costs decrease with increasing circuit speeds due to shorter running times. An increase in costs is experienced when using logic faster than 4.0 ns, and is caused by the required switch to stripline and ground-plane techniques. This will result in added expense in packaging and layout.

The enclosed individual device specifications show that MECL II is optimized for economy when computer operating time is compared with packaging and layout costs.

MECL II

GENERAL INFORMATION SECTION

SYSTEM CHARACTERISTICS

MECL II provides several important systems features. A noise immunity-power dissipation trade-off is possible by varying the supply voltage of the system. Figures 1 and 2 show the OR and NOR transfer characteristics of typical MECL II gates as the supply voltage is varied. For example, noise immunity may be increased by 0.100 V by increasing the supply voltage to −6.0 V, which increases power dissipation by 35%.

Figures 3 through 7 illustrate the typical characteristics of MECL II versus temperature and supply voltage changes. There is minimal change in system operating characteristics for ±10% supply variation. The largest change is observed at 125°C and elevated supply voltages, where the gates will be operating into the saturation region which significantly reduces operating speeds.

For driving long lines with MECL II, or interfacing between systems that have a large difference in operating temperature, balanced twisted-pair lines are recommended. The differential output of a MECL gate drives the line. The far end is terminated in the characteristic impedance of the line and received by a differential amplifier. (See the discussion with MC1020/MC1220 Quad Line Receiver.) This method yields 1.0 V or better noise immunity at a very low impedance.

A significant feature of MECL II is its low generated noise and cross-talk in a system. The output rise and fall times are approximately the same as the propagation delay times, minimizing capacitive cross-talk. The noise immunity as a percentage of logic swing is also larger than standard saturated logic. The very low logic currents switched in the lines also appreciably reduce inductive cross-talk. If line lengths are kept short with respect to the fastest rise or fall time of noise, then the line is effectively clamped to the 15-ohm output impedance of the gate. This then requires considerable energy to overcome the voltage noise immunity of the gate. MECL II also shows a significant improvement over saturated logic rejection of noise and voltage variations due to poor regulation on the supply line.

FIGURE 1 - TYPICAL "OR" TRANSFER CHARACTERISTICS

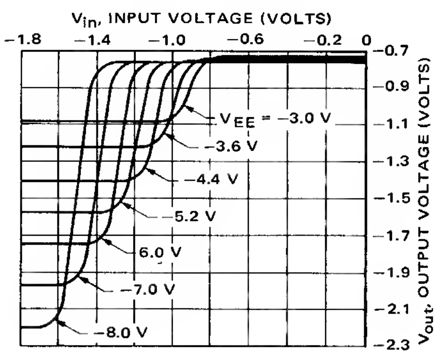


FIGURE 2 - TYPICAL "NOR" TRANSFER CHARACTERISTICS

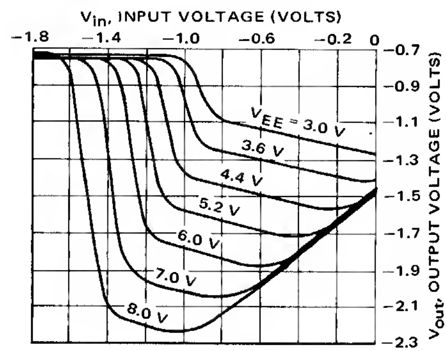


FIGURE 3 - RISE TIME versus TEMPERATURE AND SUPPLY VOLTAGE

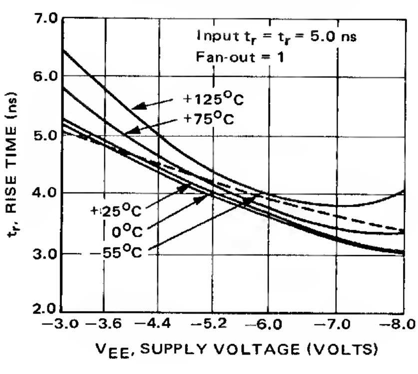


FIGURE 4 - FALL TIME versus TEMPERATURE AND SUPPLY VOLTAGE

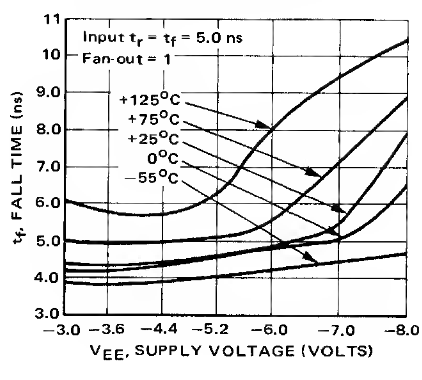


FIGURE 5 - PROPAGATION DELAY t_{pd+} versus TEMPERATURE AND SUPPLY VOLTAGE

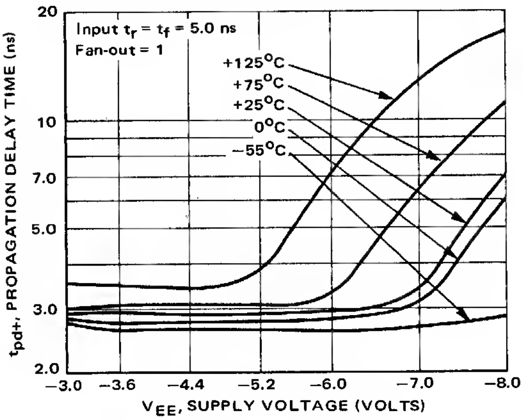


FIGURE 6 - PROPAGATION DELAY t_{pd-} versus TEMPERATURE AND SUPPLY VOLTAGE

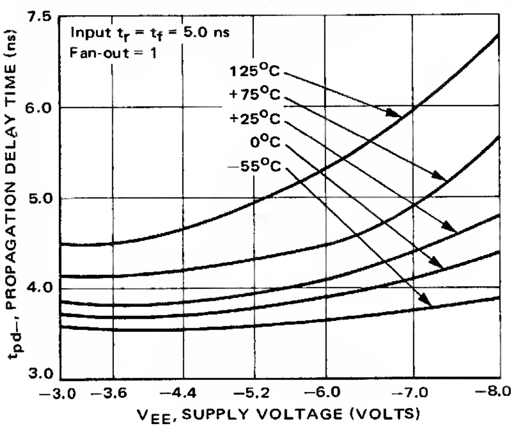
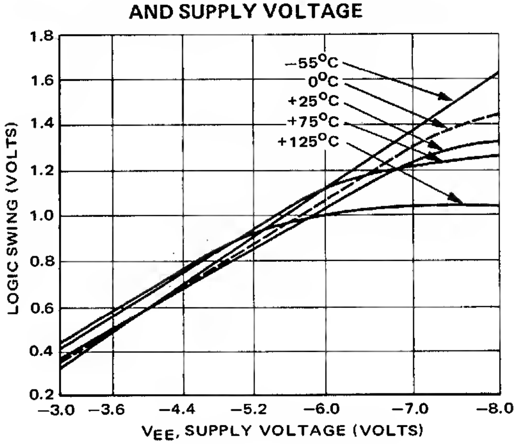


FIGURE 7 - LOGIC SWING versus TEMPERATURE AND SUPPLY VOLTAGE

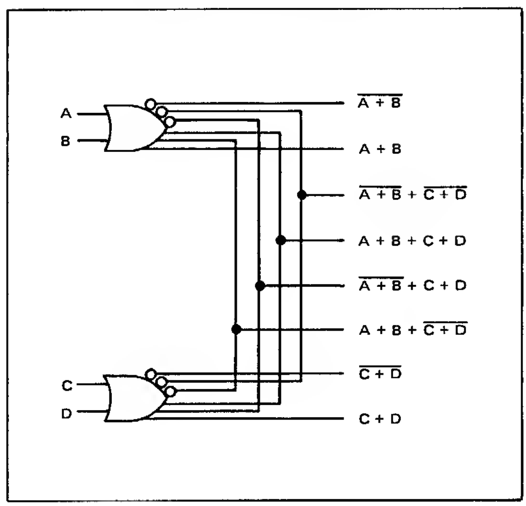


GENERAL DESIGN AND SYSTEM LAYOUT RULES

"OR"ING FEATURES

The outputs of several gates may be tied together to perform the Wired-OR function. A recommended maximum of 15 outputs should be ORed together if high-speed operation is desired. If speed is not a system requirement, a greater number of outputs may be ORed together. One pulldown resistor per Wired-OR function is recommended as a power saving feature. Two pulldowns result in appreciably better fall times with high capacitance loads. The high logic level noise immunity is reduced by a negligible amount. Three pulldown resistors reduce noise immunity typically by 50 mV and therefore are not generally recommended. As separate gates drive the Wired-OR output to the high level, approximately 3.0 mA current will be switched through the interconnecting leads with a rise time as short as 3.0 ns. To maintain the very low crosstalk advantages of MECL, it is not recommended that Wired-OR be employed on a computer back-plane but be restricted to printed circuit cards.

FIGURE 8 - EXAMPLE OF MULTIPLE OUTPUT GATE INTERCONNECTIONS



UNUSED INPUTS

All unused inputs must be tied to V_{EE} for reliable system operation. As seen from the gate input characteristics (Figure 11), the input impedance of a gate is very high when at a low-level voltage. Any leakage to the input capacitance of the gate will gradually build up a voltage on the input lead. This may affect noise imunity of the gate or hinder switching characteristics at low repetition rates. Returning the unused inputs to V_{EE} insures no build-up of voltage, and a noise immunity dependent only upon the inputs used. The emitter-base breakdown voltage of the transistors used is in excess of −6.5 V and will not start to clamp the voltage across the differential pair current source until a V_{EE} greater than −8.0 V is applied to a gate, nor will device failure occur since base current is limited internally. For most evaluation and breadboarding purposes, unused inputs may be left open with negligible difference in results.

MECL II

GENERAL INFORMATION SECTION

FAN-IN

A maximum fan-in of 20 is recommended for high-speed operation. Greatar fan-in may ba employed if fast propagation delay, rise, and fall times are not required. Further discussion is found on the data sheets for the MC1024/MC1224 Dual 2-Input Gates and the MC1025/MC1225 Dual Expanders.

V_{BB} SUPPLY

None of the MECL II devices require an external V_{BB} or reference supply, however V_{BB} has been brought out externally on the MC1017/MC1217 and MC1018/MC1218 translators for those who may require it. To maintain noise margin levels on MECL II, the maximum recommended load current for V_{BB} is 1.0 mA.

SYSTEM LAYOUT

As rise and fall times decrease, more restrictions are required on system layout. Standard MECL II exhibits typical rise, fall, and propagation delay times of 4.0 ns, but due to process and layout variations these may go as low as 3.0 ns. MECL II has been designed to be as fast as practical without requiring non-standard layout techniques such as ground planes on printed circuit boards. Two-sided printed circuit cards are still satisfactory for 3.0 ns rise times, especially since MECL draws constant current from the power supply.

Reflections that occur on high-impedance unterminated lines are a function of logic rise and/or fall times. For example, reflections can be a problem with 1.0 ns rise time and high-impedance wire lengths greater than three inches. For MECL II, maximum wire length of 12 inches is recommended. Wire length of 36 inches or more may be driven if a small ferrite bead is slipped over the wire. The ferrite bead attenuates the high-frequency components of the fast rise or fall times and therefore damps out overshoot, ringing, and reflections. Also if a wire is run adjacent to a ground plane, effective inductance per unit length may be reduced by one-half that observed when the wire is a couple of inches above the ground plane. When long wires are being driven, a recommended fan-in of one should be employed at the receiving end. Higher fan-in increases the mismatch of high impedance wires. See the discussion in Application Note AN-277 which gives methods of reducing overshoot to acceptable levels where both long leads and high fan-in are employed. Long leads and high fan-out and fan-in are less of a problem on a printed circuit board where high width-to-thickness ratios of the printed leads greatly reduce inductance. High-speed clock drivers (2.0 ns) can be used satisfactorily on two-sided printed circuit boards if the layout is designed properly.

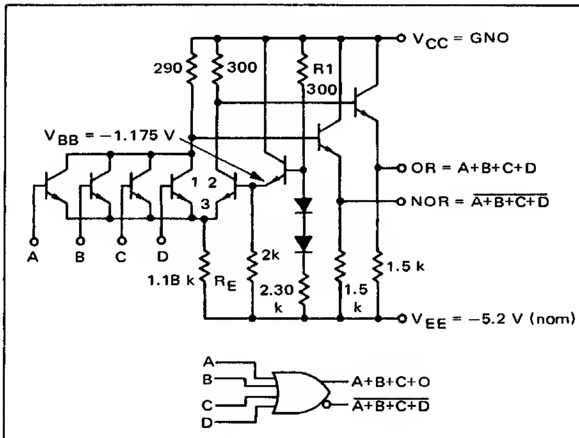
CLOCK DISTRIBUTION

Clock distribution is one of the largest system problems. Where large high-speed clock networks are required, a balanced twisted pair line is recommended for clock distribution. A gate such as the MC1001/MC1201 and the MC1020/MC1220 Quad Line Receiver make an excellent combination for distributing the clock throughout a system at frequencies to 50 MHz. (See the MC1020/MC1220 data sheet for further detail.) This method allows control of clock skew time and offers 1.0 V or better noise immunity regardless of line length.

DEFINITIONS

e_g	Generator inputs to test circuit.
I_{BL}	Base leakage current of a MECL expander input when at V_{EE}.
I_C	Total power supply current drawn from the positive supply by the test unit.
I_{CEX}	Total collector leakage current exhibited by the gate expander when all inputs are at the negative supply potential.
I_E	Total power supply current drawn from the test unit by the negative power supply.
I_F	Forward diode current drawn from an input of a saturated logic-to-MECL translator when that input is at ground potential.
I_{in}	Current drawn by the input of the test unit when a maximum logical "1" ($V_{IH\ max}$) is applied at that input.
I_L	Load current that is applied through a MECL circuit output when measuring the output "1" level voltage.
I_{OH}	Load current that is applied through a saturating output of a translator when measuring the output "1" level.
I_{OL}	Load current that is applied through a saturating output of a translator when measuring the output "0" level.
I_{out}	Output current.
I_R	Reverse current drawn from a transistor input of the test unit when V_{EE} is applied at that input.
I_{SC}	Short-circuit current drawn from a translator saturating output when that output is at ground potential.
t_f	Time required for the output pulse to go more negative from its 90% point to its 10% point.
t_{pd}, $t_{x\pm y\pm}$	Propagation delay time from the 50% point of the input waveform at pin x (falling edge noted by – or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by – or rising edge noted by +).
t_r	Time required for the output pulse to go more positive from its 10% point to its 90% point.
TP_{in}	Test point at input of unit under test.
TP_{out}	Test point at output of unit under test.
V_{BB}	Bias reference supply voltage (–1.175 V nominal at 25°C).
V_{BE}	Base-to-emitter voltage drop of a transistor.
V_{CB}	Collector-to-base voltage drop of a transistor.
V_{CC}	Most positiva power supply voltage for a circuit.
V_{EE}	Most negative power supply voltage for a circuit.
V_{in}	Input voltage.
$V_{IH\ max}$	Maximum input logical "1" level voltage.
$V_{IH\ min}$	Minimum input logical "1" level (threshold) voltage.
$V_{IL\ max}$	Maximum input logical "0" level (threshold) voltage.
$V_{IL\ min}$	Minimum input logical "0" level voltage.
V_L	Latch voltage of a dc flip-flop.
$V_{OH\ max}$	Maximum output "1" or high-level voltage.
$V_{OH\ min}$	Minimum output "1" or high-level voltage.
$V_{OL\ max}$	Maximum output "0" or low-level voltage.
$V_{OL\ min}$	Minimum output "0" or low-level voltage.
V_{out}	Output voltage.
V_{max}	Maximum positive supply voltage.

FIGURE 9 - BASIC MECL II GATE



THE BASIC MECL II LOGIC GATE

Each digital integrated circuit family is built around a basic circuit which determines the general characteristics of the family. The basic MECL II gate is evaluated in terms of circuit operation, transfer characteristics, noise margin, speed, component tolerances, and logic flexibility.

CIRCUIT OPERATION

Figure 9 illustrates a 4-input OR-NOR MECL II gate; Figure 10 depicts MECL II transfer characteristics and specification points. Typical operating voltages are V_{CC} = ground and $V_{EE} = -5.2$ V. The internal bias (V_{BB}) is designed for a nominal −1.175 V in reference to V_{CC}. When the gate inputs are all at a low level ($V_{in} \leqslant V_{IL\ max}$) the input transistors will not be conducting current and the V_{BB} transistor will act as an emitter follower. At 25°C the V_{BE}-drop of a silicon integrated transistor averages around 0.750 V for base currents within the nominal operating region. Therefore the voltage at point 3 in Figure 9 is V_{BB} − 0.750 V or −1.925 V. This potential establishes an I_E of 2.77 mA through the 1.18 k-ohm emitter resistor. I_E also causes a drop of 0.830 V across the 300-ohm collector resistor. The OR output is then obtained through an emitter follower which drops the output voltage to a nominal −1.580 V, which is a logic "0" or low logic level. The base of the NOR output transistor is essentially at 0 V, yielding an output of −0.750 V or the nominal "1" logic level.

If one or more of the gate inputs is switched to a high level ($V_{in} \geqslant V_{IH\ min}$), the current from point 2 to point 3 will switch from point 1 to point 3. Point 3 is now at −1.500 V resulting in an I_E of 3.14 mA which causes a drop of 0.900 V across the 290-ohm resistor. The nominal NOR output voltage is then −1.650 V or 0.070 V lower than the OR output. The reasons for this are seen from the transfer characteristics shown in Figure 10. Observing the NOR transfer characteristics as V_I increases from $V_{IL\ min}$ to $V_{IL\ max}$, it is seen that the output remains at a high level. For V_I increasing from $V_{IL\ max}$ to $V_{IH\ min}$, the NOR output will switch to a low level. Then as the input continues more positive than $V_{IH\ min}$, the output will continue more negative with a slope of about −0.24. This is caused by the input collector node going more negative as V_I goes more positive. If the input is increased above $V_{IH\ max}$, saturation will be reached at an input of about −0.40 V. Beyond this point, the base-collector junction is forward biased and the collector voltage will increase with an increasing input level. The nominal NOR low-level output is designed to be more negative than the nominal OR low-level output, to assure that at an input of $V_{IH\ min}$ the output is still more negative than $V_{OL\ max}$. Thus equal noise margins may be guaranteed for OR and NOR outputs.

The transfer characteristics (Figure10) show that MECL II operating levels are well below the point at which the gate starts to saturate. The saturation temperature for MECL II devices is nominally 140°C ambient. Since the transistors stay out of the saturation region, current mode is inherently the fastest form of logic obtainable. Typically gates exhibit an average propagation delay of 4.0 ns when wired into a system.

The differential input of the MECL gate offers several advantages. Input impedance is high due to the emitter follower inputs. A worst-case current of 100 μA is guaranteed. (See Figure 11 for input characteristics.) The voltage gain and transfer characteristics are practically independent of transistor parameters. The input thresholds are determined effectively by the internal V_{BB} due to the V_{BE} match of integrated circuit transistors. The collectors of the differential amplifier provide the complementary outputs at essentially the same propagation delay time. The differential input is also responsible for common mode rejection of power supply variations.

FIGURE 10 - MECL II TRANSFER CHARACTERISTICS AND SPECIFICATION POINTS

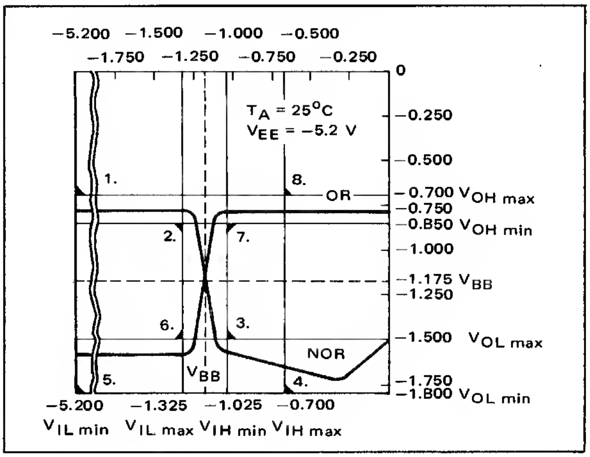
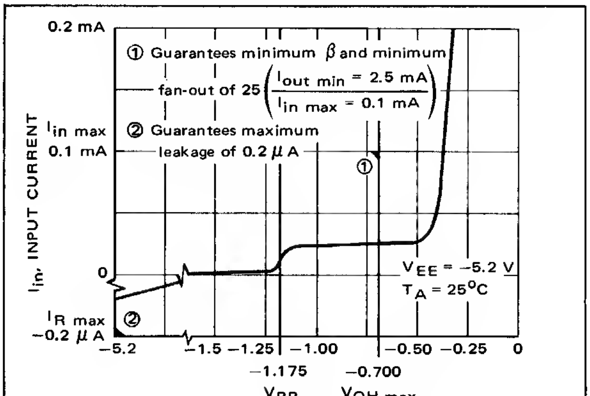


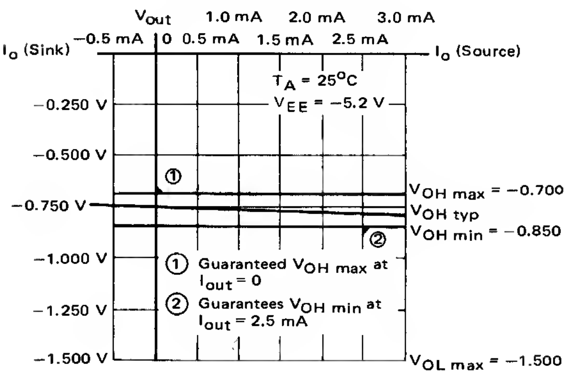
FIGURE 11 - TYPICAL INPUT VOLTAGE versus INPUT CURRENT



The emitter follower outputs offer low output impedance. Typically 15 ohms or less is measured, while a worst-case impedance of 20 ohms should be considered for any design requirements. See Figure 12 for output characteristics and specification points. The emitter follower outputs also permit the positive Wired-OR function to be obtained by tying outputs together.

Logic "0" levels in the MECL II gate are determined by resistor ratios rather than absolute values of resistance. Ratios can be held to within ±.5% while absolute values can vary by ±20%. This is a significant advantage in MECL processing. The transistors used in MECL II gates have a typical β of 150. Circuit restrictions on β are much wider than normal processing variations which yields another processing advantage. One processing step – that of gold-doping – is eliminated since the transistors operate in the non-saturating mode.

FIGURE 12 - TYPICAL OUTPUT VOLTAGE versus OUTPUT CURRENT



NOISE MARGIN

Noise margin may be defined as the difference between a worst-case logic level and the worst-case threshold closest to that logic level. The threshold point is sometimes defined as the point on a transfer characteristic curve where the slope is 1/1 indicating unity gain. For MECL II a more conservative threshold is defined as the worst-case input voltage ($V_{IH\ min}$ or $V_{IL\ max}$) for which the output is still within specified limits. Another method of testing noise immunity is obtained by cascading worst-case gates and testing to the minimum "noise" input that will just propagate through the gates. This method is more indicative of actual system operation, and is often referred to as "system noise immunity". The method corresponds to driving the gate into the active region until the output reaches a worst-case V_{BB} level which could then propagate through another gate. This method yields at least 0.040 V greater worst-case noise margin than the test methods employed, but it is very difficult to implement. Typical propagation noise immunity is 0.350 V for MECL II.

Figure 13 lists the worst-case limits for the basic MECL II family. Noise margin is easily obtained by subtracting $V_{IH\ min}$ from $V_{OH\ min}$ for high-level noise margin, and $V_{OL\ max}$ from $V_{IL\ max}$ for low-level noise margin. As seen from Figure 13, 0.175 V worst-case noise margin is guaranteed at all temperatures. Gates with higher guaranteed noise margin can be obtained by selection or special order. All noise specifications are also internally guard-banded to minimize correlation problems (a factor which also adds to actual system noise immunity). The worst-case "system noise immunity" (for noise to propagate through two or more worst-case gates) that can be measured with MECL II is 0.050 V greater than that specified in the brochure. For example, it will take more than 0.225 V of "noise" to propagate through MECL II gates specified at 0.175 V noise margin. The question often arises as to system noise margin with gates of different temperatures and power supply voltages driving one another. Figure 13 also lists the worst-case change in logic levels and threshold levels with a change in supply voltage. It is seen that the "1" logic levels are effectively independent of power supply voltage, the threshold level variance is less than 1/8 the change in V_{EE}, and the worst-case "0" logic level change is 1/4 of the V_{EE} change. These changes illustrate the common-mode rejection of power supply variations exhibited by MECL II. It may be shown that a MECL II system will operate with a ±30% variation in supply voltage, but it is recommended that a maximum variation of ±20% from the design nominal of –5.2 V be allowed. Supply variations of ±10% show negligible effect on system performance.

Figure 14 illustrates two worst-case system noise margin calculations with the data from Figure 13. It is seen that a system with a ±5% change in power supply voltage and 100°C temperature differential will still operate with worst-case devices.

Noise immunity is specified only for logic inputs. In system applications noise at both the V_{CC} and the V_{EE} nodes must be considered. The logical "1" levels in MECL II are one diode drop more negative than V_{CC}. Therefore V_{CC} noise immunity is basically the same as logic input noise immunity. In actual measurements, V_{CC} noise immunity is about 0.030 V higher than if the noise were imposed directly on a logic input. V_{EE} noise immunity is typically greater than 1.5 V due to the common-mode rejection of the basic gate.

POWER SUPPLY CONNECTIONS

Ground is usually the most stable and lowest impedance source in a system. For this reason, V_{CC} is usually at ground potential in a MECL system while V_{EE} is the supply voltage. Another advantage of having V_{CC} as ground is that an output may be shorted to ground without drawing high current. If an output is accidentally shorted to V_{EE}, no permanent damage will result. If an output remains shorted for long periods of time (especially with values of V_{EE} greater than –5.2 V), permanent degradation may result due to excessive chip temperatures. The output of high-speed MECL II devices such as the clock driver should not be shorted to V_{EE} due to its very low output impedance.

Nominal power dissipation of the MECL II circuit is 15 mW for the basic gate, 14 mW for each emitter follower pull-down resistor, and 18 mW for the built-in bias driver. Since MECL II devices are built of various combinations of the above, power dissipation per package and logic function can vary widely. For example, a single gate with six output pull-down resistors and a bias driver dissipates 120 mW, while a quad 2-input gate without pull-

FIGURE 13 - MECL II WORST-CASE LEVELS

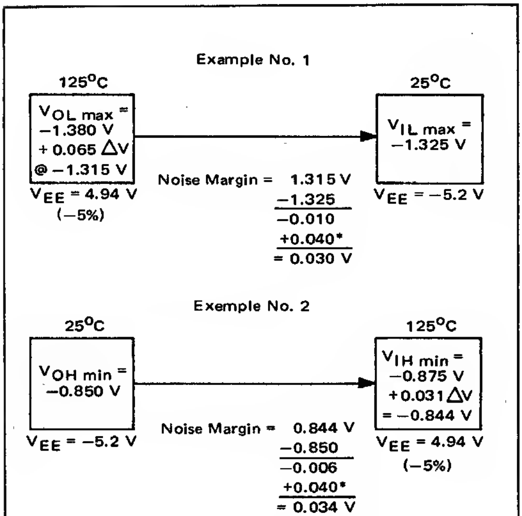
VOLTAGE LEVEL	AMBIENT TEMPERATURE				
	125°C	75°C	25°C	0°C	–55°C
$V_{IH\ max}$	–0.535	–0.600	–0.700	–0.735	–0.825
$V_{OH\ max}$	–0.535	–0.600	–0.700	–0.735	–0.825
$V_{OH\ min}$	–0.700	–0.775	–0.850	–0.895	–0.990
$V_{IH\ min}$	–0.875	–0.950	–1.025	–1.070	–1.165
$V_{IL\ max}$	–1.205	–1.260	–1.325	–1.350	–1.405
$V_{OL\ max}$	–1.380	–1.440	–1.500	–1.525	–1.580
$V_{OL\ min}$	–1.720	–1.760	–1.800	–1.830	–1.890
$V_{IL\ min}$	$< V_{EE}$	$< V_{EE}$	$< V_{EE}$	$< V_{EE}$	$< V_{EE}$

$$\frac{\Delta V_{OH}}{\Delta V_{EE}} = 0.015 \text{ max} \qquad \frac{\Delta(V_{IH\ min}, V_{IL\ max})}{\Delta V_{EE}} = \begin{matrix} 0.110 \text{ min} \\ 0.115 \text{ nom} \\ 0.120 \text{ max} \end{matrix}$$

$$\frac{\Delta(V_{OL\ max}, V_{OL\ min})}{\Delta V_{EE}} = \begin{matrix} 0.210 \text{ min} \\ 0.230 \text{ nom} \\ 0.250 \text{ max} \end{matrix}$$

down resistors and with a single bias driver dissipates only 20 mW per gate. Normalized power dissipation curves versus temperature and supply voltages are shown in Figure 15. Power dissipation for system design should be 80% of the value calculated from the I_E maximum values specified on the various data sheets. Nominal power dissipation is lower (75% of the maximum value specified).

FIGURE 14 - EXAMPLES OF WORST CASE NOISE MARGINS IN A MECL II SYSTEM



*40 mV is the minimum noise immunity gained before noise can actually propagate through worst-case getes.

Calculations shown ere for gates with 175 mV minimum noise margin. Gates with 200 mV minimum noise margin may also be specified; this would add 25 mV to the above calculations.

DC LOADING CONSIDERATIONS

Worst-case fan-out specifications are obtained from Figures 11 and 12. With a worst-case input current of 100 μA and a minimum output current of 2.5 mA for a $V_{OH\,min}$ level, a fan-out of 25 is guaranteed. Figure 16 illustrates the typical input characteristics of a MECL II gate versus temperature and a wide excursion of input voltage. The output dc loading characteristics of MECL II are shown in Figure 17 for loads that greatly exceed normal operation. It may be observed from the curves that one MECL II gate could typically drive more than a thousand other gates before noise immunity dropped below 0.100 V. It is obvious that loading restrictions are normally ac rather than dc. The heaviest loading occurs under Wired-OR conditions. If only one pull-down resistor is used (recommended as a power saving feature), the dc loading is the same as for normal conditions. If two pull-down resistors are employed, an additional current of 3.6 mA maximum is drawn at V_{EE} = −5.2 V and T_A = 25°C. $V_{OH\,min}$ is specified at 2.5 mA load current, but the worst-case pull-down resistor draws an additional 1.1 mA. A worst-case output impedance of 20 ohms would then give an additional drop of 0.022 V. If the Wired-OR also drives a nominal fan-out, the output may drop 0.025 V below $V_{OH\,min}$ which subtracts 0.025 V from the worst-case noise margin. For this reason a maximum of two pull-down resistors is recommended for worst-case system design. It should be noted that two pull-down resistors appreciably decrease fall time under high capacitance loading. Typically three pull-down resistors (an additional load of 6.0 mA) would give a V_{OH} of 0.850 V, which is $V_{OH\,min}$.

AC LOADING CONSIDERATIONS

The input capacitance of a MECL II gate averages 3.3 pF. Since in any system stray capacitance is also present, a typical value of 5.0 pF per fan-out should be used for design purposes. A fan-out of 15 MECL II gates is than roughly equivalent to 75 pF, while a fan-out of 20 gates would be approximately 100 pF. These figures may be easily decreased with careful layout techniques.

FIGURE 15 - NORMALIZED POWER DISSIPATION versus TEMPERATURE AND SUPPLY VOLTAGE

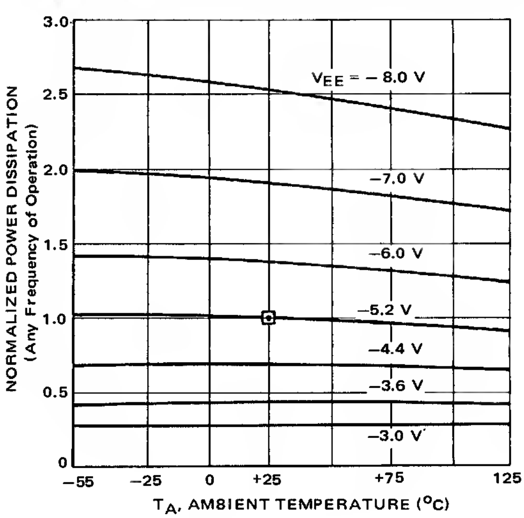


FIGURE 16 - INPUT CURRENT versus INPUT VOLTAGE AND TEMPERATURE

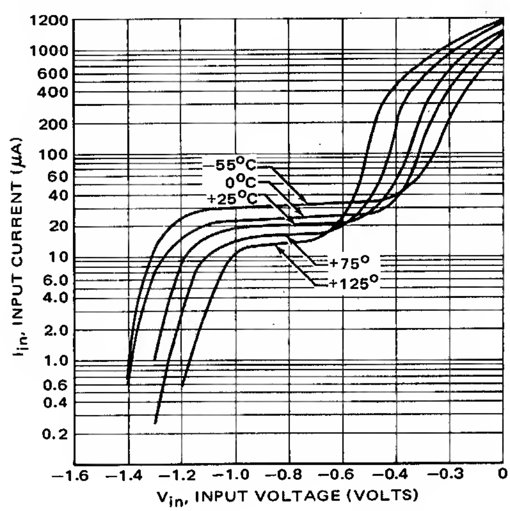
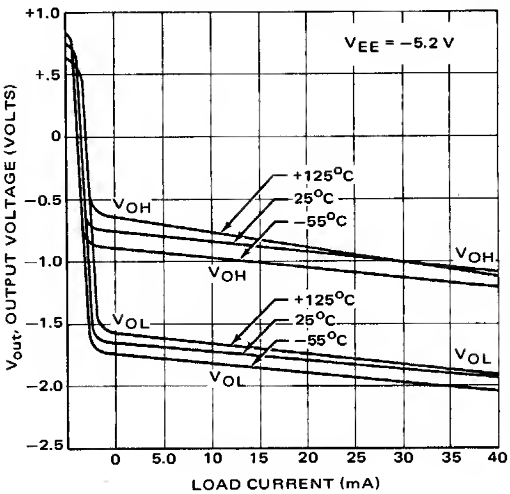


FIGURE 17 - TYPICAL OUTPUT VOLTAGES versus LOAD CURRENT
(Ambient Temperature)



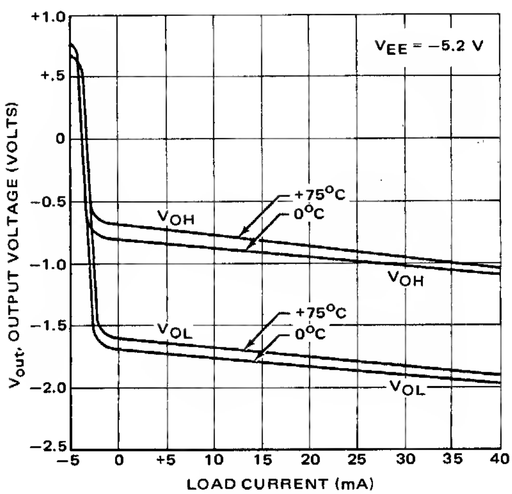


FIGURE 18 - RISE TIME versus LOADING AND TEMPERATURE

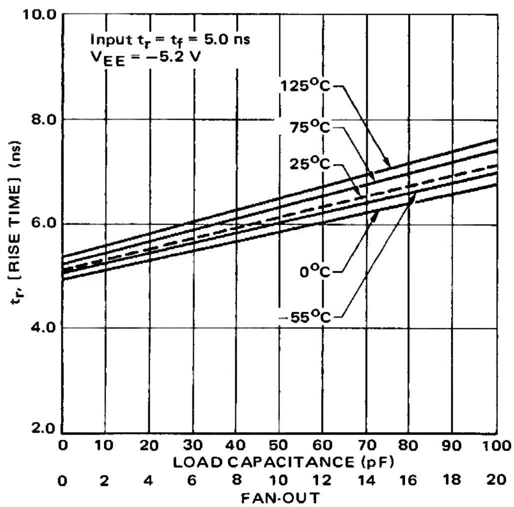
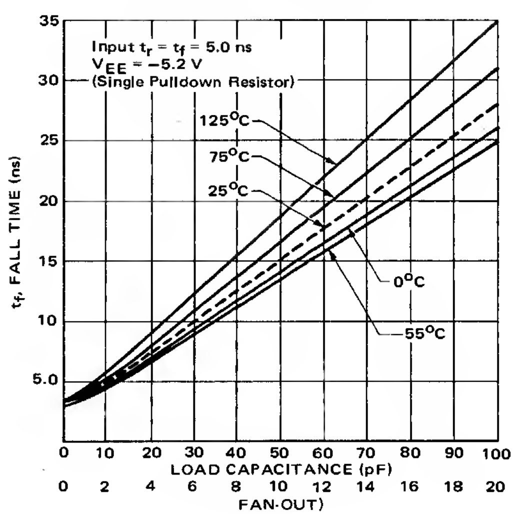


FIGURE 19 - FALL TIME versus LOADING AND TEMPERATURE
(Single Pulldown Resistor)



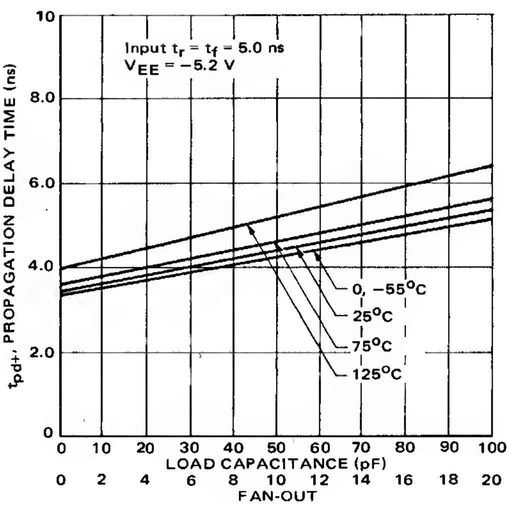
SWITCHING TIMES

Figures 18 through 21 give typical rise, fall, and propagation delay times versus loading and temperature. The slow fall times and t_{pd-} are caused by the relatively long R-C time constant of the emitter pull-down resistor and the load capacitance. The fall time, t_f, may be calculated as 0.2 RC, where R is the value of the pull-down resistor (in kΩ) and C is the external load capacitance (in pF). For example, with a 100 pF load and a 1.5 k-ohm internal resistor, the fall time is approximately 30 ns. The increase in t_{pd-} over the delay at no load is very closely obtained by 0.1 RC. At no load, t_{pd-} is approximately 3.5 ns, and 0.1 RC with a 100 pF load is 15 ns, giving a total of 18.5 ns for t_{pd-}. The RC time constant of the load may be reduced significantly (for high capacitance) by paralleling an external resistance with the load to V_{EE}.

MECL II

GENERAL INFORMATION SECTION

FIGURE 20 - PROPAGATION DELAY t_{pd+} versus LOADING AND TEMPERATURE



THERMAL CHARACTERISTICS

The junction temperature of the integrated circuit is closely related to its long term operational characteristics; therefore, an accurate estimate of the junction temperature of the various circuit components must be made before the circuit designer can predict the expected reliability of his system. Motorola is including sufficient information in this section to permit the user of MECL II to estimate worst-case junction temperatures if he can estimate accurately the ambient or case temperatures and the operating circuit's power drain.

The average temperature at the junction region is a function of the systems ability to remove the heat generated in the circuit from the junction regions to the ambient or equivalent heat sink. The basic formula for converting calculated power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA})$$

or

$$T_J = T_A + P_D (\theta_{JA})$$

where

T_A = ambient temperature
P_D = calculated power dissipation
θ_{JC} = thermal resistance, junction to case
θ_{CA} = thermal resistance, case to ambient
θ_{JA} = thermal resistance, junction to ambient.

The worst-case rated thermal resistance values for Motorola's integrated circuit packages are found in Table 1. Figures 22, 23, and 24 are variations of the same derating curve. Figure 22, for instance, plots the maximum permissible package power handling capability as a function of ambient temperature when the maximum permissible junction is at 150°C (plastic package) and 175°C (ceramic flat package). Figure 23 plots worst-case junction temperature as a function of power dissipated for the two ambient temperatures, 75°C and 125°C. Figure 24 plots the junction temperature as a function of power drain when the case temperature is held constant. These figures have been developed using the worst-case thermal resistance values found in Table 1.

FIGURE 21 - PROPAGATION DELAY t_{pd-} versus LOADING AND TEMPERATURE

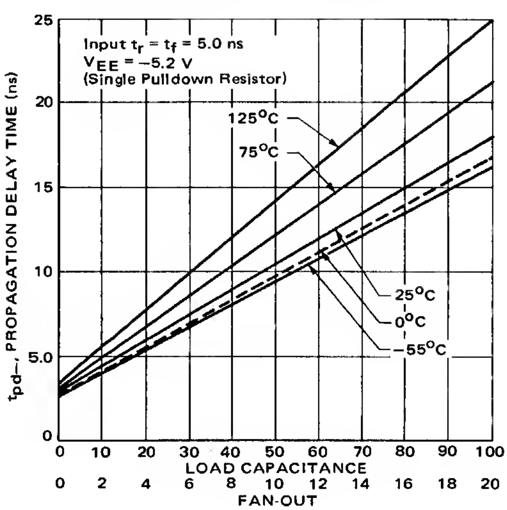


FIGURE 22 - AMBIENT TEMPERATURE DERATING CURVE

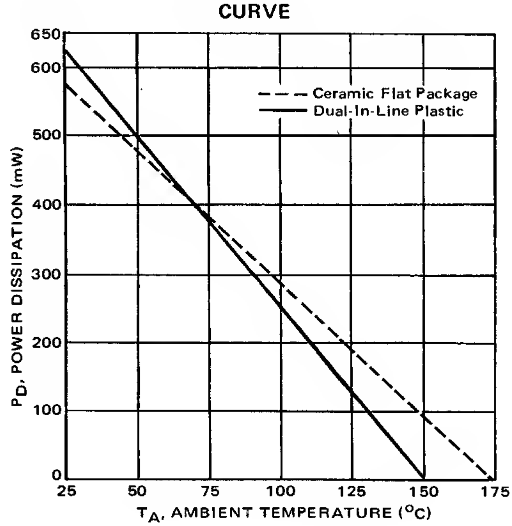


FIGURE 23 - JUNCTION TEMPERATURE DERATING CURVE USING AMBIENT TEMPERATURE

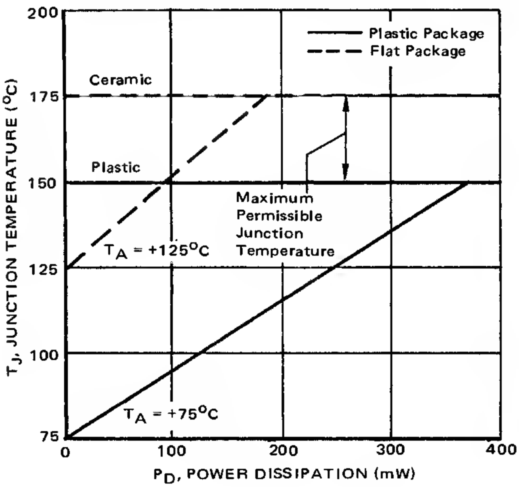


FIGURE 24 - JUNCTION TEMPERATURE DERATING CURVE USING CASE TEMPERATURE

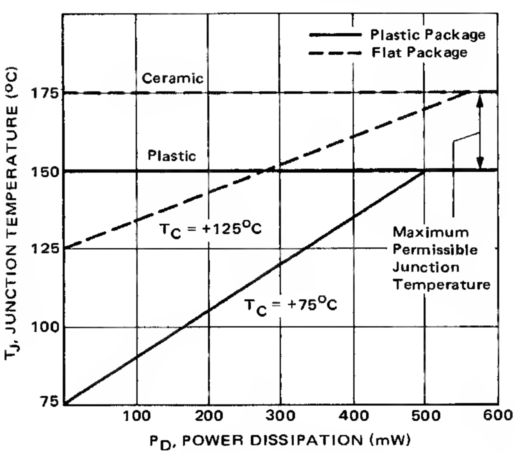


TABLE 1 - WORST-CASE THERMAL RESISTANCE OF INTEGRATED CIRCUIT PACKAGES

PACKAGE	θ_{JA} JUNCTION TO AMBIENT	θ_{JC} JUNCTION TO CASE
Ceramic Flat Package 14 lead ¼ x ¼ inch	0.26°C/mW	0.090°C/mW
Plastic 14 lead dual-in-line	0.20°C/mW	0.15°C/mW

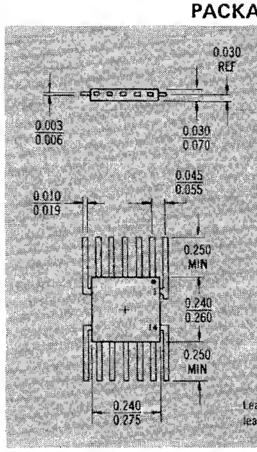
MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−10	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current	Io	20	mAdc
Storage Temperature Range MC1000 / MC1200	T_{stg}	−55 to +125 / −65 to +175	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range MC1000 / MC1200	T_A	0 to +75 / −55 to +125	°C
AC Fan-In (Expandable Gates)	m	20	—
AC Fan-Out* (Gates and Flip-Flops)	n	15	—

*Although a minimum dc fan-out of 25 is guaranteed in each electrical specification, it is recommended that the maximum ac fan-out of 15 be used for high-speed operation.

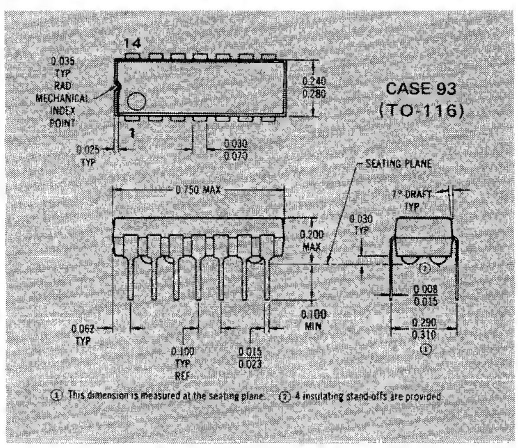
PACKAGING

The MC1000 Series is available in the dual in-line plastic package, case 93 (add suffix "P" to basic type number) and the MC1200 Series in the TO-86 ceramic flat package, case 83 (suffix "F").



CASE 83
(TO-86)

Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.



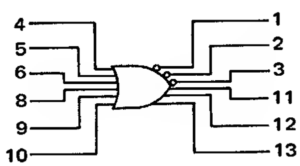
CASE 93
(TO-116)

MC1001 thru MC1003
MC1201 thru MC1203

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.

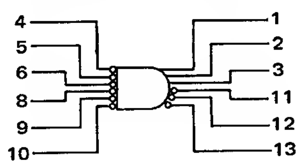
POSITIVE LOGIC



$1 = \overline{4 + 5 + 6 + 8 + 9 + 10}$

$11 = 4 + 5 + 6 + 8 + 9 + 10$

NEGATIVE LOGIC



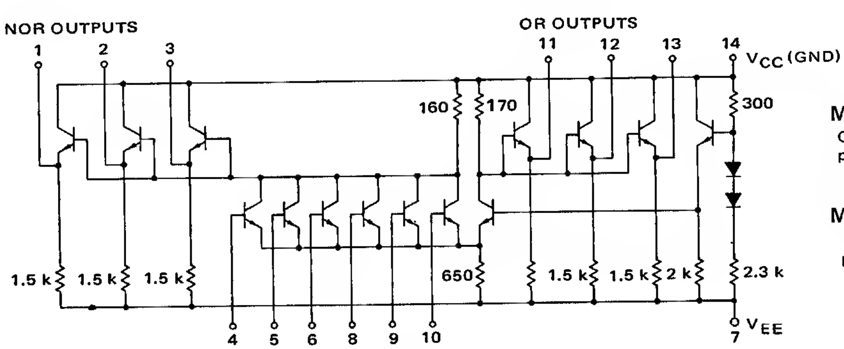
$1 = \overline{4 \cdot 5 \cdot 6 \cdot 8 \cdot 9 \cdot 10}$

$11 = 4 \cdot 5 \cdot 6 \cdot 8 \cdot 9 \cdot 10$

DC Input Loading Factor = 2
DC Output Loading Factor = 25

Power Dissipation = MC1001/MC1201 – 115 mW typical
MC1002/MC1202 – 80 mW typical
MC1003/MC1203 – 40 mW typical

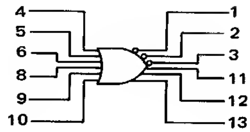
MC1001/MC1201 CIRCUIT SCHEMATIC



MC1002/MC1202
Omit NOR output pulldown resistors

MC1003/MC1203
Omit all output pulldown resistors

Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Outputs without pull-down resistors are tested with a 1.5 kΩ resistor to V_{EE}.

Characteristic	Symbol	Pin Under Test	MC1201-1203 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1001-1003 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7														
MC1201/MC1001		↓	-	-	-	32	-	-	mAdc	-	-	-	32	-	-	mAdc
MC1202/MC1002		↓	-	-	-	22	-	-	↓	-	-	-	22	-	-	↓
MC1203/MC1003		↓	-	-	-	11	-	-	↓	-	-	-	11	-	-	↓
Input Current	I_{in}	4	-	-	-	200	-	-	µAdc	-	-	-	200	-	-	µAdc
		5	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		6	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		8	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		9	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		10	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	µAdc	-	-	-	0.2	-	1.0	µAdc
"NOR" Logical "1" Output Voltage	V_{OH}‡	1, 2, 3†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	1, 2, 3†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"OR" Logical "1" Output Voltage‡	V_{OH}‡	11, 12, 13†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"OR" Logical "0" Output Voltage	V_{OL}	11, 12, 13†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{4+1-}	1	4.0	7.5	4.0	7.0	6.0	9.0	ns	4.0	7.0	4.0	7.0	5.0	8.0	ns
	t_{4-1+}	1	↓	↓	↓	↓	6.0	9.0	↓	↓	↓	↓	↓	↓	↓	↓
	t_{4+11+}	11	↓	↓	↓	↓	5.0	9.0	↓	↓	↓	↓	↓	↓	↓	↓
	t_{4-11-}	11	↓	↓	↓	↓	6.0	9.0	↓	↓	↓	↓	↓	↓	↓	↓
(Fan-Out = 15)	t_{4+1-}	1	18	-	18	-	22	-	↓	18	-	18	-	20	-	↓
	t_{4-1+}	1	6.0	-	6.0	-	8.0	-	↓	6.0	-	6.0	-	7.0	-	↓
	t_{4+11+}	11	4.0	-	4.0	-	6.0	-	↓	4.0	-	4.0	-	5.0	-	↓
	t_{4-11-}	11	13	-	13	-	17	-	↓	13	-	13	-	15	-	↓
Rise Time (Fan-Out = 3)	t_{1+}	1	5.0	8.0	5.0	7.5	6.0	9.0	↓	5.0	7.5	5.0	7.5	5.5	8.0	↓
	t_{11+}	11	4.0	7.0	4.0	6.5	5.0	8.0	↓	4.0	6.5	4.0	6.5	4.5	7.0	↓
Fall Time (Fan-Out = 3)	t_{1-}	1	6.0	8.5	6.0	8.0	7.0	10	↓	6.0	8.0	6.0	8.0	6.5	9.0	↓
	t_{11-}	11	6.0	8.0	6.0	8.0	7.0	10	↓	6.0	8.0	6.0	8.0	6.5	9.0	↓

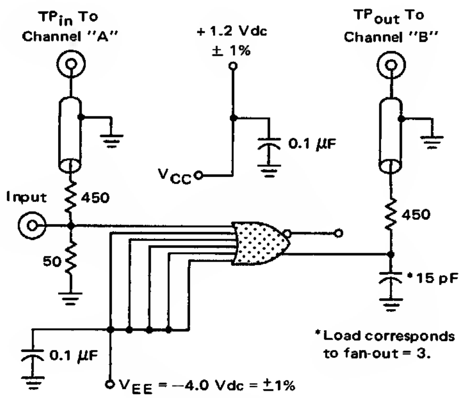
* Individually test each input using the pin connections shown.
† Individually test each output listed using the pin connections shown.
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA). I_L applied to output under test.

	@Test Temperature	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L
		TEST VOLTAGE/CURRENT VALUES				
		Vdc ±1.0%				mAdc
MC1201-1203	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1001-1003	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

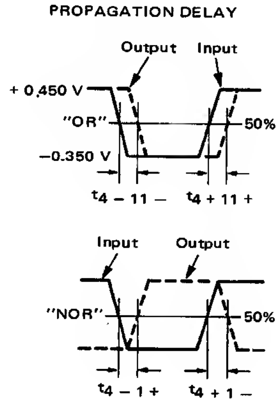
TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

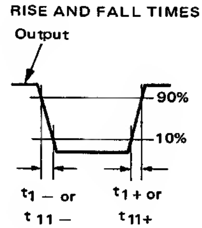
Characteristic	Symbol	Pin Under Test	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7						
MC1201/MC1001			-	-	-	4, 5, 6, 7, 8, 9, 10	-	14
MC1202/MC1002			-	-	-		-	
MC1203/MC1003			-	-	-		-	
Input Current	I_{in}	4	-	-	4	5, 6, 7, 8, 9, 10	-	14
		5	-	-	5	4, 6, 7, 8, 9, 10	-	
		6	-	-	6	4, 5, 7, 8, 9, 10	-	
		8	-	-	8	4, 5, 6, 7, 9, 10	-	
		9	-	-	9	4, 5, 6, 7, 8, 10	-	
		10	-	-	10	4, 5, 6, 7, 8, 9		
Input Leakage Current	I_R	Inputs*	-	-	-	4, 5, 6, 7, 8, 9, 10	-	14
"NOR" Logical "1" Output Voltage	V_{OH}‡	1, 2, 3†	4	-	-	5, 6, 7, 8, 9, 10	‡	14
			5	-	-	4, 6, 7, 8, 9, 10		
			6	-	-	4, 5, 7, 8, 9, 10		
			8	-	-	4, 5, 6, 7, 9, 10		
			9	-	-	4, 5, 6, 7, 8, 10		
			10	-	-	4, 5, 6, 7, 8, 9		
"NOR" Logical "0" Output Voltage	V_{OL}	1, 2, 3†	-	4	-	5, 6, 7, 8, 9, 10	-	14
			-	5	-	4, 6, 7, 8, 9, 10	-	
			-	6	-	4, 5, 7, 8, 9, 10	-	
			-	8	-	4, 5, 6, 7, 9, 10	-	
			-	9	-	4, 5, 6, 7, 8, 10	-	
			-	10	-	4, 5, 6, 7, 8, 9	-	
"OR" Logical "1" Output Voltage‡	V_{OH}‡	11, 12, 13†	-	4	-	5, 6, 7, 8, 9, 10	‡	14
			-	5	-	4, 6, 7, 8, 9, 10		
			-	6	-	4, 5, 7, 8, 9, 10		
			-	8	-	4, 5, 6, 7, 9, 10		
			-	9	-	4, 5, 6, 7, 8, 10		
			-	10	-	4, 5, 6, 7, 8, 9		
"OR" Logical "0" Output Voltage	V_{OL}	11, 12, 13†	4	-	-	5, 6, 7, 8, 9, 10	-	14
			5	-	-	4, 6, 7, 8, 9, 10	-	
			6	-	-	4, 5, 7, 8, 9, 10	-	
			8	-	-	4, 5, 6, 7, 9, 10	-	
			9	-	-	4, 5, 6, 7, 8, 10	-	
			10	-	-	4, 5, 6, 7, 8, 9	-	
			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2V)
Switching Times Propagation Delay (Fan-Out = 3)	t_{4+1-}	1	4	1	-	5, 6, 7, 8, 9, 10	-	14
	t_{4-1+}	1		1	-		-	
	t_{4+11+}	11		11	-		-	
	t_{4-11-}	11		11	-		-	
(Fan-Out = 15)	t_{4+1-}	1		1	-		-	
	t_{4-1+}	1		1	-		-	
	t_{4+11+}	11		11	-		-	
	t_{4-11-}	11		11	-		-	
Rise Time (Fan-Out = 3)	t_{1+}	1		1	-		-	
	t_{11+}	11		11	-		-	
Fall Time (Fan-Out = 3)	t_{1-}	1		1	-		-	
	t_{11-}	11		11	-		-	

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input pulse t_r and t_f = 5.0 ± 0.5 ns





Switching waveforms shown for pulse in on pin 4 and pulse out on pins 1 and 11, however all other input-output combinations will meet the limits specified.

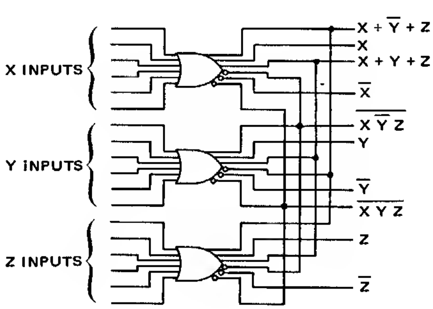
APPLICATIONS INFORMATION

The MC1001-1003/MC1201-1203 6-input OR/NOR gates are extremely useful in generating multiple wired-OR logic functions since six independent outputs are provided. (An example is shown in Figure 1.) The gate performs well as a clock driver with the multiple outputs which result in three times the normal fan-out for a given clock waveform. If twisted pair lines are being used for clock distribution in a system, the gate will drive three independent twisted pair lines, each with the same clock waveform.

An output impedance of about 2 ohms is obtained if three OR or NOR outputs are tied together. This provides an excellent 50-ohm driving capability. The 50-ohm line or coax should be terminated in its characteristic impedance to a nominal −2.0 V. This prevents excessively high output current that would pull the logic "1" level below nominal (see Figure 2).

FIGURE 1 - MECL II "WIRED OR" FEATURE

EXAMPLE SHOWN FOR ONE POSSIBLE COMBINATION OF OUTPUTS



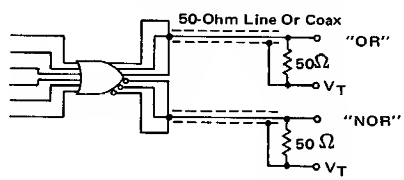
WHERE:
X = f (Six Variables)
Y = f (Six Variables)
Z = f (Six Variables)

t_{pd} Average = 4.0 ns
Total Power = 200 mW

NOTE:
All Outputs That Are Used Require An Internal or External Pulldown Resistor.

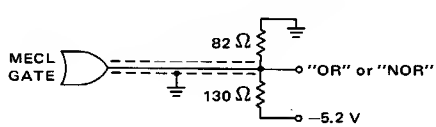
FIGURE 2 - MC1003/MC1203 AS A 50-OHM DRIVER WITH NOMINAL MECL LOGIC LEVELS

50-OHM TERMINATION TO SEPARATE NEGATIVE VOLTAGE



$V_T \approx -2.0$ V Well Bypassed To Ground

50 OHM TERMINATION TO MECL POWER SUPPLY



Output Logic Swing ≈ 0.8 V
Typical Gate Propagation Delay = 4.0 ns
Typical Rise Time At 50-Ohm Load = 7.0 ns
Typical Fall Time At 50-Ohm Load = 7.0 ns

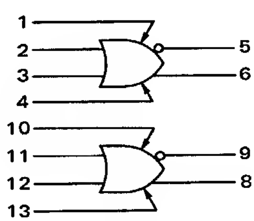
MC1024
MC1224

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

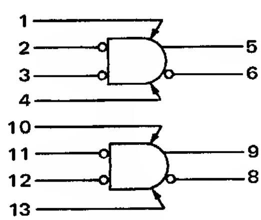
Expandable inputs are available on pins 1, 4 and 10, 13 as shown in the circuit schematic.

POSITIVE LOGIC

NEGATIVE LOGIC



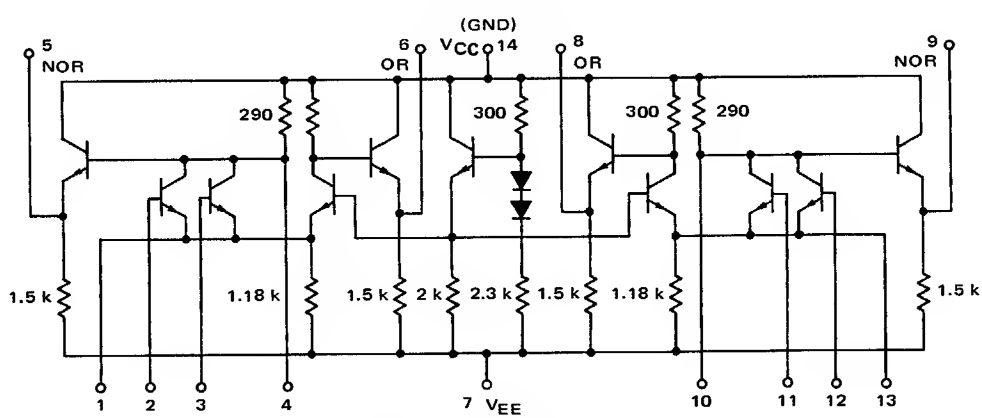
$5 = \overline{2+3}$
$6 = 2+3$



$5 = \overline{2 \cdot 3}$
$6 = 2 \cdot 3$

DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 95 mW typical

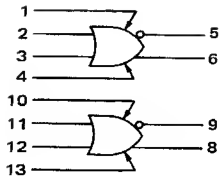
CIRCUIT SCHEMATIC



Resistor values are nominal.

MC1024, MC1224 (continued)

ELECTRICAL CHARACTERISTICS



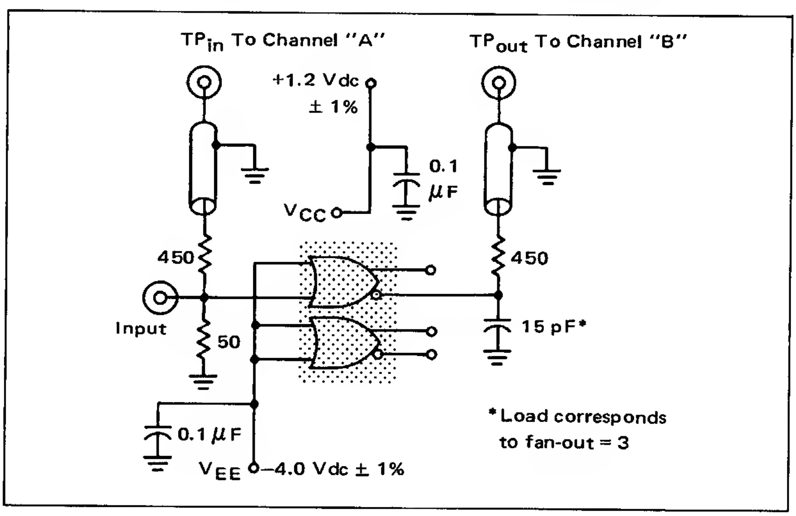
Test procedures are shown for only one gate.
The other gate is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1224 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1024 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	26	-	-	mAdc	-	-	-	26	-	-	mAdc
Input Current	I_{in}	2 3	- -	- -	- -	100 100	- -	- -	µAdc µAdc	- -	- -	- -	100 100	- -	- -	µAdc µAdc
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	µAdc	-	-	-	0.2	-	1.0	µAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	5 5	-0.990 -0.990	-0.825 -0.825	-0.850 -0.850	-0.700 -0.700	-0.700 -0.700	-0.530 -0.530	Vdc Vdc	-0.895 -0.895	-0.740 -0.740	-0.850 -0.850	-0.700 -0.700	-0.775 -0.775	-0.615 -0.615	Vdc Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	5 5	-1.890 -1.890	-1.580 -1.580	-1.800 -1.800	-1.500 -1.500	-1.720 -1.720	-1.380 -1.380	Vdc Vdc	-1.830 -1.830	-1.525 -1.525	-1.800 -1.800	-1.500 -1.500	-1.760 -1.760	-1.435 -1.435	Vdc Vdc
"OR" Logical "1" Output Voltage‡	V_{OH}‡	6 6	-0.990 -0.990	-0.825 -0.825	-0.850 -0.850	-0.700 -0.700	-0.700 -0.700	-0.530 -0.530	Vdc Vdc	-0.895 -0.895	-0.740 -0.740	-0.850 -0.850	-0.700 -0.700	-0.775 -0.775	-0.615 -0.615	Vdc Vdc
"OR" Logical "0" Output Voltage	V_{OL}	6 6	-1.890 -1.890	-1.580 -1.580	-1.800 -1.800	-1.500 -1.500	-1.720 -1.720	-1.380 -1.380	Vdc Vdc	-1.830 -1.830	-1.525 -1.525	-1.800 -1.800	-1.500 -1.500	-1.760 -1.760	-1.435 -1.435	Vdc Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{2+5-}	5	5.0	7.0	5.0	7.0	6.5	9.0	ns	5.0	7.0	5.0	7.0	6.0	8.0	ns
	t_{2-5+}	5	4.0	7.5	4.0	7.5	5.5	9.0		4.0	7.5	4.0	7.5	5.0	8.5	
	t_{2+6+}	6	4.0	7.5	4.0	7.0	5.5	8.5		4.0	7.0	4.0	7.0	5.0	8.0	
	t_{2-6-}	6	4.0	7.0	4.0	7.0	5.5	9.0		4.0	7.0	4.0	7.0	5.0	8.0	
(Fan-Out = 15)	t_{2+5-}	5	14	-	14	-	18	-		14	-	14	-	16	-	
	t_{2-5+}	5	5.0	-	5.0	-	7.0	-		5.0	-	5.0	-	6.0	-	
	t_{2+6+}	6	6.0	-	6.0	-	8.0	-		6.0	-	6.0	-	7.0	-	
	t_{2-6-}	6	13	-	13	-	17	-		13	-	13	-	15	-	
Rise Time (Fan-Out = 3)	t_{5+}	5	5.0	7.5	5.0	7.5	6.0	9.0		5.0	7.5	5.0	7.5	5.0	8.0	
	t_{6+}	6	4.0	7.0	4.0	6.5	5.5	8.0		4.0	6.5	4.0	6.5	5.0	7.0	
Fall Time (Fan-Out = 3)	t_{5-}	5	5.0	8.5	5.0	8.0	6.0	10		5.0	8.0	5.0	8.0	5.5	9.0	
	t_{6-}	6	5.0	8.0	5.0	8.0	7.0	10		5.0	8.0	5.0	8.0	6.0	9.0	

* Individually test each input using the pin connections shown.

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

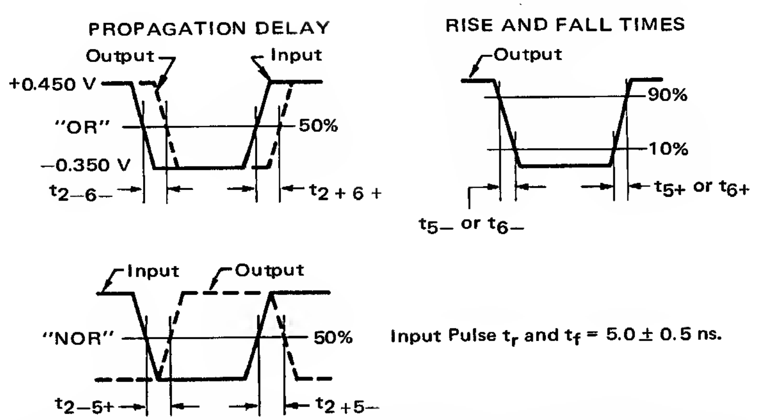
SWITCHING TIME TEST CIRCUIT @ 25°C



	@Test Temperature	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L
		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0%				mAdc
MC1224	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1024	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Characteristic	Symbol	Pin Under Test	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	2,3,7,11,12	-	14
Input Current	I_{in}	2 3	- -	- -	2 3	3,7,11,12 2,7,11,12	- -	14 14
Input Leakage Current	I_R	Inputs*	-	-	-	2,3,7,11,12	-	14
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	5 5	2 3	- -	- -	3,7,11,12 2,7,11,12	5 5	14 14
"NOR" Logical "0" Output Voltage	V_{OL}	5 5	- -	2 3	- -	3,7,11,12 2,7,11,12	- -	14 14
"OR" Logical "1" Output Voltage‡	V_{OH}‡	6 6	- -	2 3	- -	3,7,11,12 2,7,11,12	6 6	14 14
"OR" Logical "0" Output Voltage	V_{OL}	6 6	2 3	- -	- -	3,7,11,12 2,7,11,12	- -	14 14
Switching Times			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2 V)
Propagation Delay (Fan-Out = 3)	t_{2+5-}	5	2	5	-	3,7,11,12	-	14
	t_{2-5+}	5		5	-		-	
	t_{2+6+}	6		6	-		-	
	t_{2-6-}	6		6	-		-	
(Fan-Out = 15)	t_{2+5-}	5		5	-		-	
	t_{2-5+}	5		5	-		-	
	t_{2+6+}	6		6	-		-	
	t_{2-6-}	6		6	-		-	
Rise Time (Fan-Out = 3)	t_{5+}	5		5	-		-	
	t_{6+}	6		6	-		-	
Fall Time (Fan-Out = 3)	t_{5-}	5		5	-		-	
	t_{6-}	6		6	-		-	



Switching waveforms shown for pulse in on pin 2 and pulse out on pins 5 and 6, however all other input-output combinations will meet the limits specified.

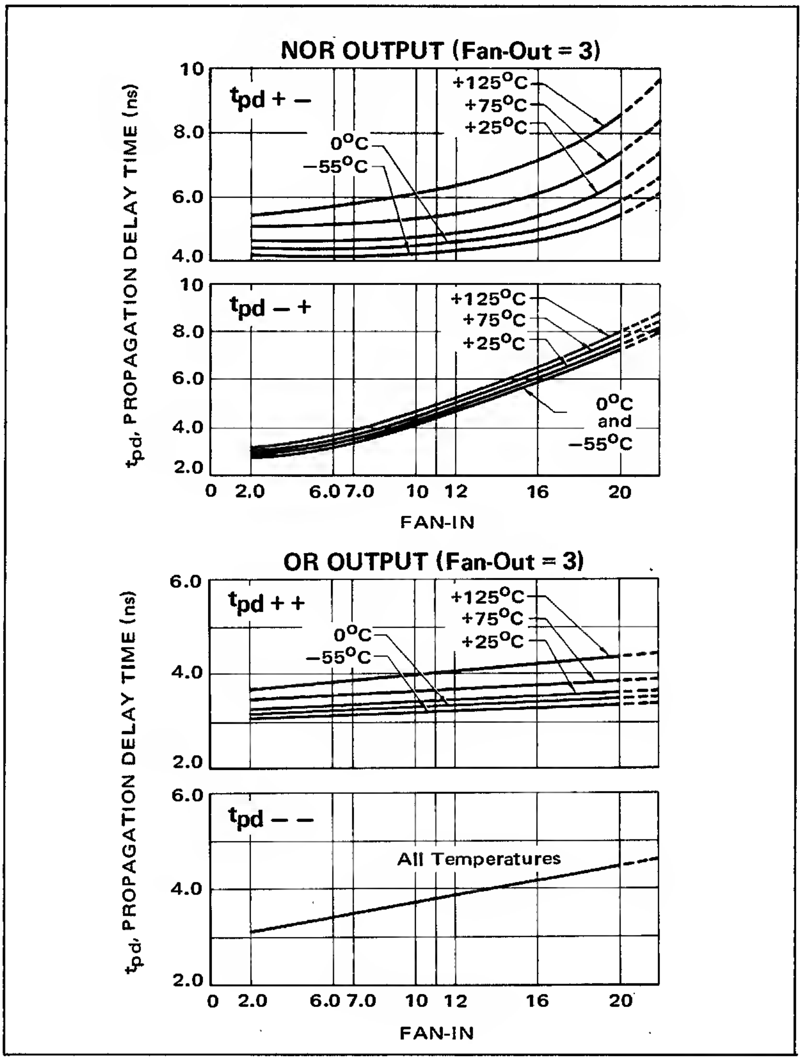
SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

The MC1024/MC1224 dual 2-input expandable OR/NOR gate provides the capability of increasing fan-in by making available the collector and emitter nodes of the standard gate. Note that complementary outputs are available, lending to circuit flexibility. By using the MC1025/MC1225 expander 6, 7, 10, 11, 12, 15, 16, or 20 gate inputs may be obtained with one or two expanders per gate. Note that as fan-in is increased, capacitance is added to the input collector node and propagation delays through the gate will increase. A maximum fan-in of 20 is recommended for high-speed operation. If high speed is not required, larger fan-ins may be utilized.

The expandable inputs allow a large fan-in NOR or NAND gate to be obtained, where power dissipation is decreased at the expense of propagation delay. The OR propagation delay times vary little with increasing fan-in since capacitance is not being added to the OR collector node. At a fan-in of 20, NOR output rise and fall times approach 20 ns, while OR output rise and fall times remain about 4.0 ns. For minimal added capacitance at the NOR collector node, lead lengths should be kept short and the circuits wired in directly rather than using sockets. Typical propagation delay curves versus fan-in and temperature are shown below.

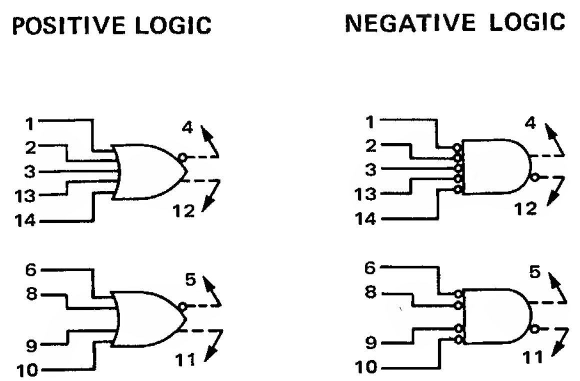
TYPICAL PROPAGATION DELAY TIMES



MC1025
MC1225

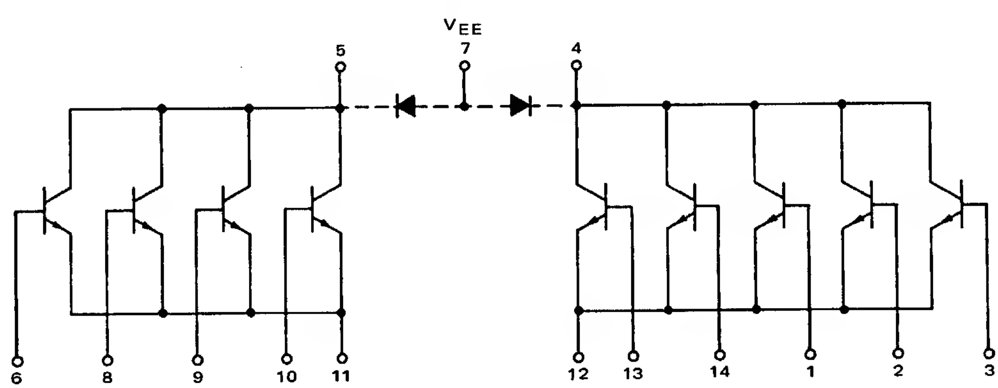
Dual expander arrays, with a 4-transistor array isolated from a 5-transistor array. The collectors and emitters from both arrays may be connected to form a 9-transistor array. With each base available, a 4, 5, or 9-input expander may be obtained.

Designed specifically for use with MC1024/MC1224 Dual 2-Input Gates.



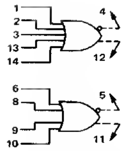
DC Input Loading Factor = 1

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in the same manner.



@ All Temperatures

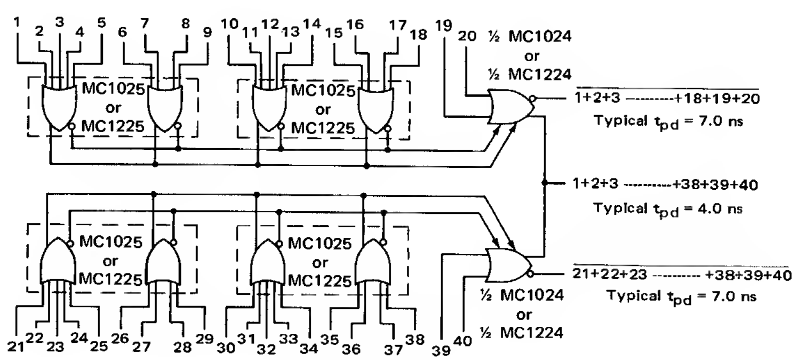
TEST VOLTAGE/CURRENT VALUES					
Vdc ±1.0%					mAdc
V_{EE}	V_{CC}	V_{BB}	V_{CB}	V_{BE}	I_E
-2.0	+2.0	-5.2	+0.7	+0.3	-1.33

			MC1225 Test Limits							MC1025 Test Limits							TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:						
		Pin Under	−55°C		+25°C		+125°C			0°C		+25°C		+75°C									
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit	V_{EE}	V_{CC}	V_{BB}	V_{CB}	V_{BE}	I_E	Gnd
Base Leakage Current	I_{BL}	1	-	0.5	-	0.5	-	2.0	μAdc	-	0.5	-	0.5	-	2.0	μAdc	11, 12	-	1	-	-	-	4, 5, 7
		2	-		-		-			-		-		-				-	2	-	-	-	
		3	-		-		-			-		-		-				-	3	-	-	-	
		13	-		-		-			-		-		-				-	13	-	-	-	
		14	-		-		-			-		-		-				-	14	-	-	-	
Collector Leakage Current	I_{CEX}	1	-	1.0	-	1.0	-	100	μAdc	-	1.0	-	1.0	-	15.0	μAdc	-	4, 5, 7	-	-	1	-	11, 12
		2	-		-		-			-		-		-			-		-	-	2	-	
		3	-		-		-			-		-		-			-		-	-	3	-	
		13	-		-		-			-		-		-			-		-	-	13	-	
		14	-		-		-			-		-		-			-		-	-	14	-	
Input Voltage	V_{BE}	12	-0.860	-0.910	-0.710	-0.760	-0.520	-0.570	Vdc	-0.760	-0.810	-0.710	-0.760	-0.610	-0.660	Vdc	-	-	-	4, 5	-	12	1, 2, 3, 13, 14

APPLICATIONS INFORMATION

The MC1025/MC1225 dual 4-5 input expander is designed to work with the MC1024/MC1224 expandable gate. The transistors are manufactured with the same buried layer process used on all MECL II devices and are typical of MECL II gate transistors. BV_{CEO} is 12 V or greater, $f_T \approx 600$ MHz, and β is typically from 100 to 150. An example of two 20-input NOR gates and a 40-input OR gate made from an MC1024/MC1224 expandable gate and four MC1025/MC1225 expanders is shown.

Two 20-input NOR gates and one 40-input OR gate generated using one MC1024/MC1224 expandable gate and four MC1025/MC1225 expanders.



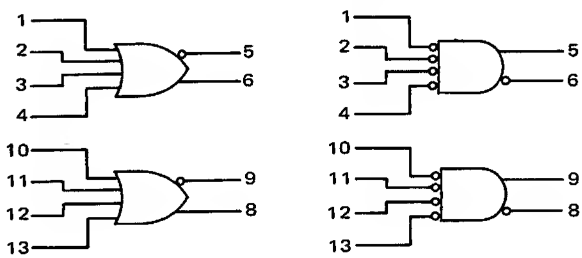
Power Dissipation = 100 mW

MC1004 thru MC1006
MC1204 thru MC1206

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.

POSITIVE LOGIC / **NEGATIVE LOGIC**



$5 = \overline{1 + 2 + 3 + 4}$

$6 = 1 + 2 + 3 + 4$

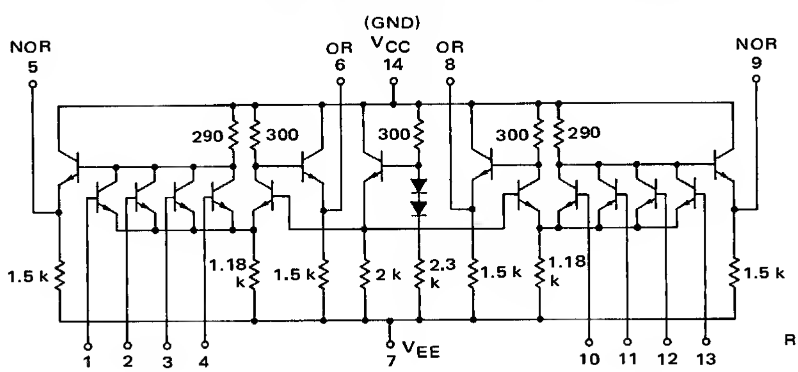
$5 = \overline{1 \cdot 2 \cdot 3 \cdot 4}$

$6 = 1 \cdot 2 \cdot 3 \cdot 4$

DC Input Loading Factor = 1
DC Output Loading Factor = 25

Power Dissipation = MC1004/MC1204 — 95 mW typical
MC1005/MC1205 — 65 mW typical
MC1006/MC1206 — 45 mW typical

MC1004/MC1204 CIRCUIT SCHEMATIC



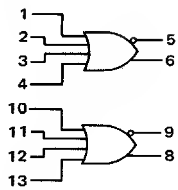
MC1005/MC1205
Omit NOR output pulldown resistors.

MC1006/MC1206
Omit all output pulldown resistors.

Resistor values are nominal.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Outputs without pulldown resistors are tested with a 1.5 kΩ resistor to V_{EE}.



Characteristic	Symbol	Pin Under Test	MC1204-1206 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1004-1006 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current MC1204/MC1004 MC1205/MC1005 MC1206/MC1006	I_E	7 ↓	- - -	- - -	- - -	26 18 12	- - -	- - -	mAdc ↓	- - -	- - -	- - -	26 18 12	- - -	- - -	mAdc ↓
Input Current	I_{in}	1 2 3 4	- - - -	- - - -	- - - -	100 ↓	- - - -	- - - -	µAdc ↓	- - - -	- - - -	- - - -	100 ↓	- - - -	- - - -	µAdc ↓
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	µAdc	-	-	-	0.2	-	1.0	µAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	5 ↓	-0.990 ↓	-0.825 ↓	-0.850 ↓	-0.700 ↓	-0.700 ↓	-0.530 ↓	Vdc ↓	-0.895 ↓	-0.740 ↓	-0.850 ↓	-0.700 ↓	-0.775 ↓	-0.615 ↓	Vdc ↓
"NOR" Logical "0" Output Voltage	V_{OL}	5 ↓	-1.890 ↓	-1.580 ↓	-1.800 ↓	-1.500 ↓	-1.720 ↓	-1.380 ↓	Vdc ↓	-1.830 ↓	-1.525 ↓	-1.800 ↓	-1.500 ↓	-1.760 ↓	-1.435 ↓	Vdc ↓
"OR" Logical "1" Output Voltage‡	V_{OH}‡	6 ↓	-0.990 ↓	-0.825 ↓	-0.850 ↓	-0.700 ↓	-0.700 ↓	-0.530 ↓	Vdc ↓	-0.895 ↓	-0.740 ↓	-0.850 ↓	-0.700 ↓	-0.775 ↓	-0.615 ↓	Vdc ↓
"OR" Logical "0" Output Voltage	V_{OL}	6 ↓	-1.890 ↓	-1.580 ↓	-1.800 ↓	-1.500 ↓	-1.720 ↓	-1.380 ↓	Vdc ↓	-1.830 ↓	-1.525 ↓	-1.800 ↓	-1.500 ↓	-1.760 ↓	-1.435 ↓	Vdc ↓
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{1+5-}	5	5.0	7.0	5.0	7.0	6.5	9.0	ns	5.0	7.0	5.0	7.0	6.0	8.0	ns
	t_{1-5+}	5	4.0	7.5	4.0	7.5	5.5	9.0	↓	4.0	7.5	4.0	7.5	5.0	8.5	↓
	t_{1+6+}	6	4.0	7.5	4.0	7.0	5.5	8.5	↓	4.0	7.0	4.0	7.0	5.0	8.0	↓
	t_{1-6-}	6	4.0	7.0	4.0	7.0	5.5	9.0	↓	4.0	7.0	4.0	7.0	5.0	8.0	↓
(Fan-Out = 15)	t_{1+5-}	5	14	-	14	-	18	-	↓	14	-	14	-	16	-	↓
	t_{1-5+}	5	5.0	-	5.0	-	7.0	-	↓	5.0	-	5.0	-	6.0	-	↓
	t_{1+6+}	6	6.0	-	6.0	-	8.0	-	↓	6.0	-	6.0	-	7.0	-	↓
	t_{1-6-}	6	13	-	13	-	17	-	↓	13	-	13	-	15	-	↓
Rise Time (Fan-Out = 3)	t_{5+}	5	5.0	7.5	5.0	7.5	6.0	9.0	↓	5.0	7.5	5.0	7.5	5.0	8.0	↓
	t_{6+}	6	4.0	7.0	4.0	6.5	5.5	8.0	↓	4.0	6.5	4.0	6.5	5.0	7.0	↓
Fall Time (Fan-Out = 3)	t_{5-}	5	5.0	8.5	5.0	8.0	6.0	10	↓	5.0	8.0	5.0	8.0	5.5	9.0	↓
	t_{6-}	6	5.0	8.0	5.0	8.0	7.0	10	↓	5.0	8.0	5.0	8.0	6.0	9.0	↓

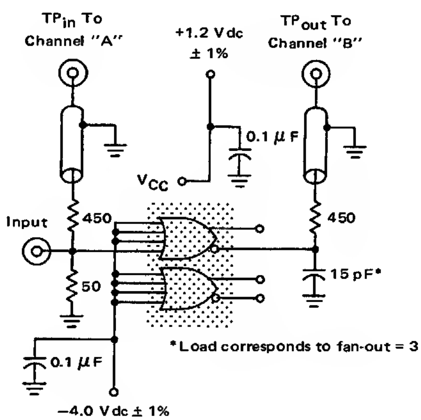
* Individually test each input using the pin connections shown. ‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0%: $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	mAdc: I_L
MC1204-1206	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1004-1006	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

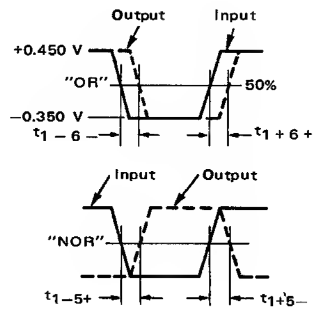
Characteristic	Symbol	Pin Under Test	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7						
MC1204/MC1004		↓	-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13	-	14
MC1205/MC1005		↓	-	-	-	↓	-	↓
MC1206/MC1006		↓	-	-	-	↓	-	↓
Input Current	I_{in}	1	-	-	1	2, 3, 4, 7, 10, 11, 12, 13	-	14
		2	-	-	2	1, 3, 4, 7, 10, 11, 12, 13	-	↓
		3	-	-	3	1, 2, 4, 7, 10, 11, 12, 13	-	↓
		4	-	-	4	1, 2, 3, 7, 10, 11, 12, 13	-	↓
Input Leakage Current	I_R	Inputs*	-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13	-	14
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	5	1	-	-	2, 3, 4, 7, 10, 11, 12, 13	5	14
		↓	2	-	-	1, 3, 4, 7, 10, 11, 12, 13	↓	↓
		↓	3	-	-	1, 2, 4, 7, 10, 11, 12, 13	↓	↓
		↓	4	-	-	1, 2, 3, 7, 10, 11, 12, 13	↓	↓
"NOR" Logical "0" Output Voltage	V_{OL}	5	-	1	-	2, 3, 4, 7, 10, 11, 12, 13	-	14
		↓	-	2	-	1, 3, 4, 7, 10, 11, 12, 13	-	↓
		↓	-	3	-	1, 2, 4, 7, 10, 11, 12, 13	-	↓
		↓	-	4	-	1, 2, 3, 7, 10, 11, 12, 13	-	↓
"OR" Logical "1" Output Voltage‡	V_{OH}‡	6	-	1	-	2, 3, 4, 7, 10, 11, 12, 13	6	14
		↓	-	2	-	1, 3, 4, 7, 10, 11, 12, 13	↓	↓
		↓	-	3	-	1, 2, 4, 7, 10, 11, 12, 13	↓	↓
		↓	-	4	-	1, 2, 3, 7, 10, 11, 12, 13	↓	↓
"OR" Logical "0" Output Voltage	V_{OL}	6	1	-	-	2, 3, 4, 7, 10, 11, 12, 13	-	14
		↓	2	-	-	1, 3, 4, 7, 10, 11, 12, 13	-	↓
		↓	3	-	-	1, 2, 4, 7, 10, 11, 12, 13	-	↓
		↓	4	-	-	1, 2, 3, 7, 10, 11, 12, 13	-	↓
			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2 V)
Switching Times Propagation Delay (Fan-Out = 3)	t_{1+5-}	5	1	5	-	2, 3, 4, 7, 10, 11, 12, 13	-	14
	t_{1-5+}	5	↓	5	-	↓	-	↓
	t_{1+6+}	6	↓	6	-	↓	-	↓
	t_{1-6-}	6	↓	6	-	↓	-	↓
(Fan-Out = 15)	t_{1+5-}	5	↓	5	-	↓	-	↓
	t_{1-5+}	5	↓	5	-	↓	-	↓
	t_{1+6+}	6	↓	6	-	↓	-	↓
	t_{1-6-}	6	↓	6	-	↓	-	↓
Rise Time (Fan-Out = 3)	t_{5+}	5	↓	5	-	↓	-	↓
	t_{6+}	6	↓	6	-	↓	-	↓
Fall Time (Fan-Out = 3)	t_{5-}	5	↓	5	-	↓	-	↓
	t_{6-}	6	↓	6	-	↓	-	↓

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

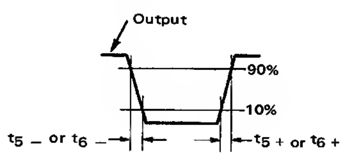


Input Pulse t_r and t_f = 5.0 ± 0.5 ns.

PROPAGATION DELAY



RISE AND FALL TIMES

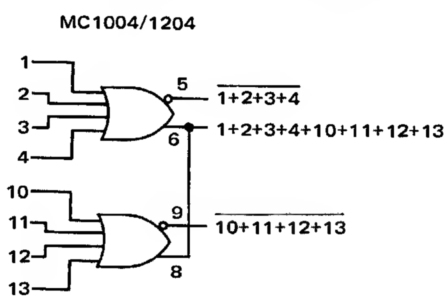


Switching waveforms shown for pulse in on pin 1 and pulse out on pins 5 and 6, however all other input-output combinations will meet the limits specified.

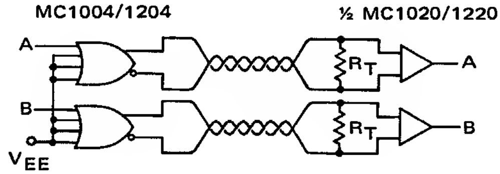
APPLICATIONS INFORMATION

The MC1004-1006/MC1204-1206 dual 4-input OR/NOR gates are very useful in generating system logic due to their flexibility. By employing negative logic on the inputs (low level of − 1.6 V is considered true), the AND/NAND logic function is obtained from the basic gate. Since complementary inputs are available in MECL system, OR/NOR-AND/NAND logic may be employed, reducing the package count in the system. An 8-input OR or AND gate is obtained by tying the OR outputs together and using positive or negative logic. The dual 4-input gate is also useful for driving two twisted pair lines where the lines must carry independent information. For a further discussion of twisted pair driving and receiving, refer to MC1020/MC1220 Line Receiver.

8-INPUT "OR" GATE (positive logic) or 8-INPUT "AND" GATE (negative logic)



DUAL 4-INPUT GATE USED TO DRIVE TWO BALANCED TWISTED PAIR LINES



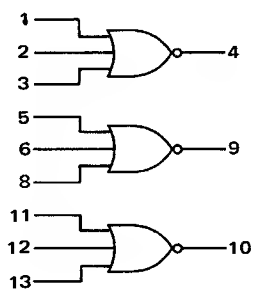
R_T IS THE TERMINATING RESISTOR. VERY LONG LEAD LENGTHS MAY BE EMPLOYED

MC1007 thru MC1009
MC1207 thru MC1209

Provide the NOR output function. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

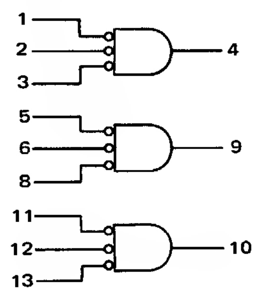
Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.

POSITIVE LOGIC



$4 = \overline{1 + 2 + 3}$

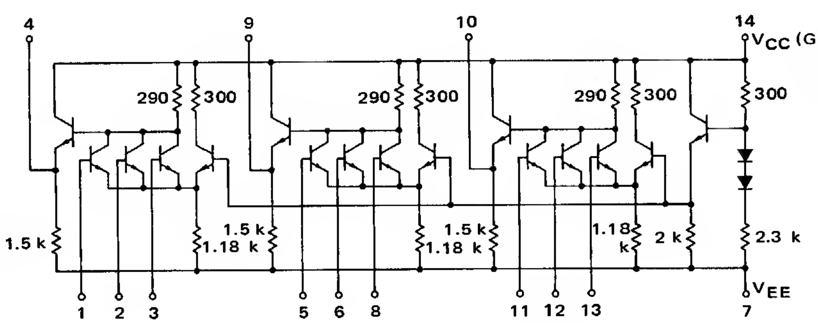
NEGATIVE LOGIC



$4 = \overline{1 \cdot 2 \cdot 3}$

DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = MC1007/MC1207 — 110 mW typical
MC1008/MC1208 — 75 mW typical
MC1009/MC1209 — 60 mW typical

MC1007/MC1207 CIRCUIT SCHEMATIC



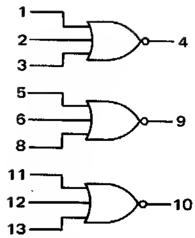
MC1008/MC1208

Omit output pulldown resistors to pins 9 and 10.

MC1009/MC1209

Omit all output pulldown resistors.

Resistor values are nominal.



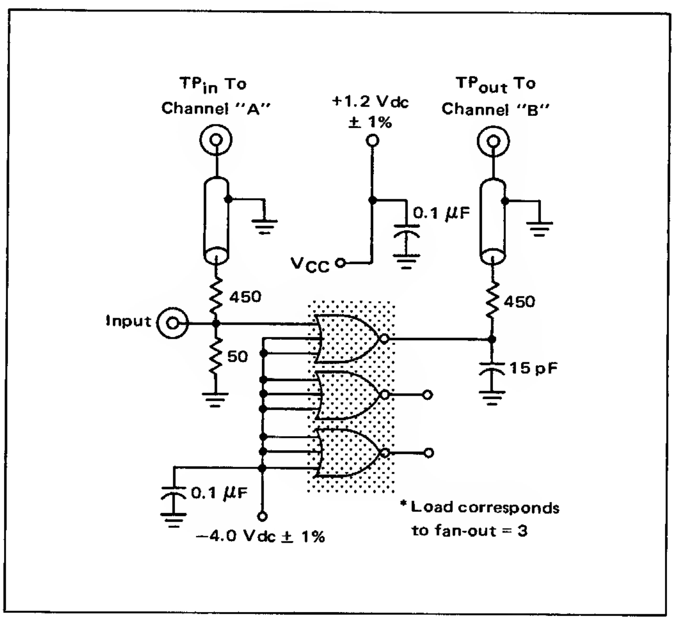
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs without pulldown resistors are tested with a 1.5 k ohm resistor to V_{EE}.

Characteristic	Symbol	Pin Under Test	MC1207-1209 Test Limits							MC1007-1009 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7														
MC1207/MC1007		↓	-	-	-	30	-	-	mAdc	-	-	-	30	-	-	mAdc
MC1208/MC1008		↓	-	-	-	20	-	-	↓	-	-	-	20	-	-	↓
MC1209/MC1009		↓	-	-	-	16	-	-	↓	-	-	-	16	-	-	↓
Input Current	I_{in}	1	-	-	-	100	-	-	µAdc	-	-	-	100	-	-	µAdc
		2	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		3	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	µAdc	-	-	-	0.2	-	1.0	µAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	4 ↓	-0.990 ↓	-0.825 ↓	-0.850 ↓	-0.700 ↓	-0.700 ↓	-0.530 ↓	Vdc ↓	-0.895 ↓	-0.740 ↓	-0.850 ↓	-0.700 ↓	-0.775 ↓	-0.615 ↓	Vdc ↓
"NOR" Logical "0" Output Voltage	V_{OL}	4 ↓	-1.890 ↓	-1.580 ↓	-1.800 ↓	-1.500 ↓	-1.720 ↓	-1.380 ↓	Vdc ↓	-1.830 ↓	-1.525 ↓	-1.800 ↓	-1.500 ↓	-1.760 ↓	-1.435 ↓	Vdc ↓
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{1+4-}	4	4.0	7.5	4.0	7.5	6.0	9.0	ns	4.0	7.5	4.0	7.5	5.0	8.5	ns
	t_{1-4+}	↓	4.0	7.0	4.0	7.0	6.0	9.0	↓	4.0	7.0	4.0	7.0	5.0	8.0	↓
(Fan-Out = 15)	t_{1+4-}	↓	18	-	18	-	22	-	↓	18	-	18	-	20	-	↓
	t_{1-4+}	↓	5.0	-	5.0	-	9.0	-	↓	5.0	-	5.0	-	7.0	-	↓
Rise Time (Fan-Out = 3)	t_{4+}	↓	5.0	7.5	5.0	7.5	6.0	9.0	↓	5.0	7.5	5.0	7.5	5.5	8.0	↓
Fall Time (Fan-Out = 3)	t_{4-}	↓	6.0	8.5	6.0	8.0	7.0	10	↓	6.0	8.0	6.0	8.0	6.0	9.0	↓

* Individually test each input using the pin connections shown.
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

SWITCHING TIME TEST CIRCUIT @ 25°C



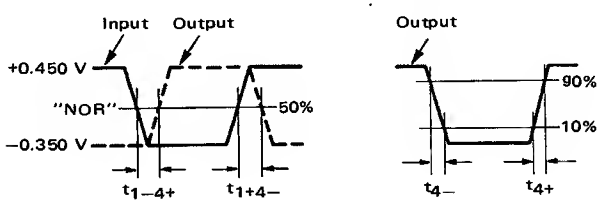
	@Test Temperature	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L
		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0%				mAdc
MC1207-1209	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1007-1009	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Characteristic	Symbol	Pin Under Test	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7				1, 2, 3, 5, 6, 7, 8, 11, 12, 13		14
MC1207/MC1007		↓	-	-	-	↓	-	↓
MC1208/MC1008		↓	-	-	-	↓	-	↓
MC1209/MC1009		↓	-	-	-	↓	-	↓
Input Current	I_{in}	1	-	-	1	2, 3, 5, 6, 7, 8, 11, 12, 13	-	14
		2	-	-	2	1, 3, 5, 6, 7, 8, 11, 12, 13	-	↓
		3	-	-	3	1, 2, 5, 6, 7, 8, 11, 12, 13	-	↓
Input Leakage Current	I_R	Inputs*	-	-	-	1, 2, 3, 5, 6, 7, 8, 11, 12, 13	-	14
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	4	1	-	-	2, 3, 5, 6, 7, 8, 11, 12, 13	4	14
		↓	2	-	-	1, 3, 5, 6, 7, 8, 11, 12, 13	↓	↓
		↓	3	-	-	1, 2, 5, 6, 7, 8, 11, 12, 13	↓	↓
"NOR" Logical "0" Output Voltage	V_{OL}	4	-	1	-	2, 3, 5, 6, 7, 8, 11, 12, 13	-	14
		↓	-	2	-	1, 3, 5, 6, 7, 8, 11, 12, 13	-	↓
		↓	-	3	-	1, 2, 5, 6, 7, 8, 11, 12, 13	-	↓
Switching Times			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2 V)
Propagation Delay (Fan-Out = 3)	t_{1+4-}	4	1	4	-	2, 3, 5, 6, 7, 8, 11, 12, 13	-	14
	t_{1-4+}	↓	↓	↓	-	↓	-	↓
(Fan-Out = 15)	t_{1+4-}	↓	↓	↓	-	↓	-	↓
	t_{1-4+}	↓	↓	↓	-	↓	-	↓
Rise Time (Fan-Out = 3)	t_{4+}	↓	↓	↓	-	↓	-	↓
Fall Time (Fan-Out = 3)	t_{4-}	↓	↓	↓	-	↓	-	↓

PROPAGATION DELAY

RISE AND FALL TIMES



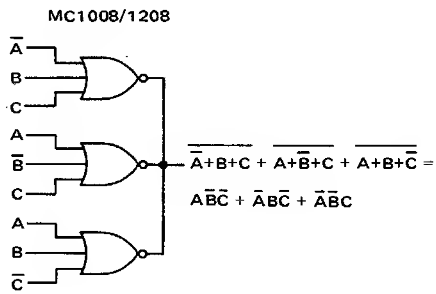
SWITCHING TIME WAVEFORMS

Switching waveforms shown for pulse in on pin 1 and pulse out on pin 4, however all other input-output combinations will meet the limits specified.

Input Pulse t_r and t_f = 5.0 ± 0.5 ns.

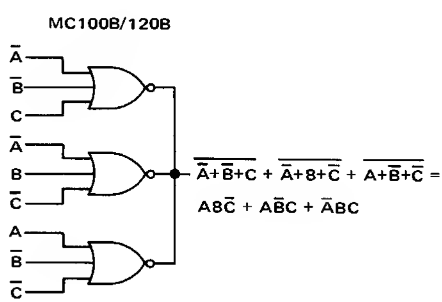
APPLICATIONS INFORMATION

The MC1007-1009/MC1207-1209 triple 3-input gates provide NOR outputs only, due to the pin limitation of the 14-lead package. The three options on the emitter follower pull-down resistors, as on all of the basic gates, provide a significant power savings when the wired-OR feature is utilized. The power dissipation of additional emitter-follower resistors and additional gates to perform the OR function is eliminated. By making liberal use of the wired-OR feature, power dissipation in a logic system may be reduced by one-half. If fast propagation delay time through a logic chain is required, an additional gate propagation delay of 4.0 to 5.0 ns is saved each time the wired-OR option is employed. Shown below are two examples of an MC1008/MC1208 with the outputs wired together.



A true output is provided if one and only one of the variables is true.

True = high logic level



A true output is provided if two and only two of the variables are true.

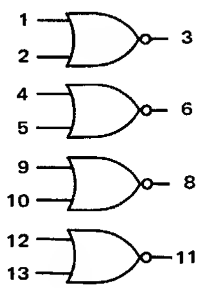
True = high logic level

MC1010 thru MC1012
MC1210 thru MC1212

Provide the NOR output function. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

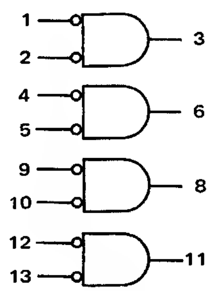
Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.

POSITIVE LOGIC



$3 = \overline{1 + 2}$

NEGATIVE LOGIC

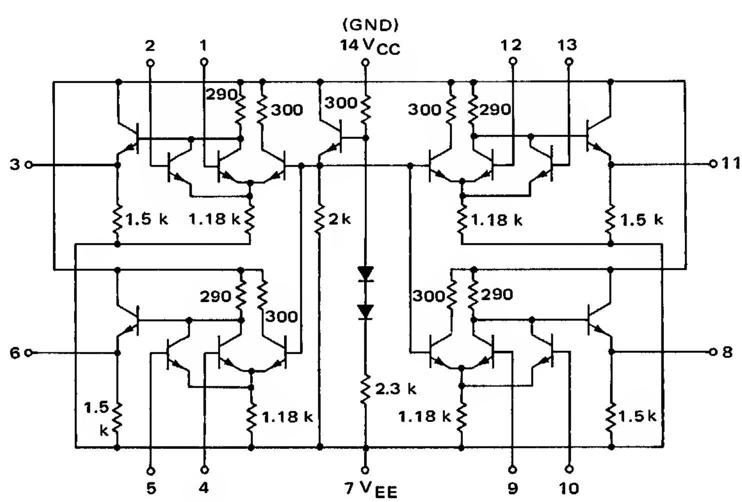


$3 = \overline{1 \cdot 2}$

DC Input Loading Factor = 1
DC Output Loading Factor = 25

Power Dissipation: MC1010/MC1210 – 115 mW typical
MC1011/MC1211 – 95 mW typical
MC1012/MC1212 – 65 mW typical

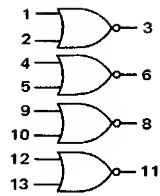
MC1010/MC1210 CIRCUIT SCHEMATIC



MC1011/MC1211
Omit pulldown resistors on pins 3 and 6

MC1012/MC1212
Omit all output pulldown resistors

Resistor values are nominal.



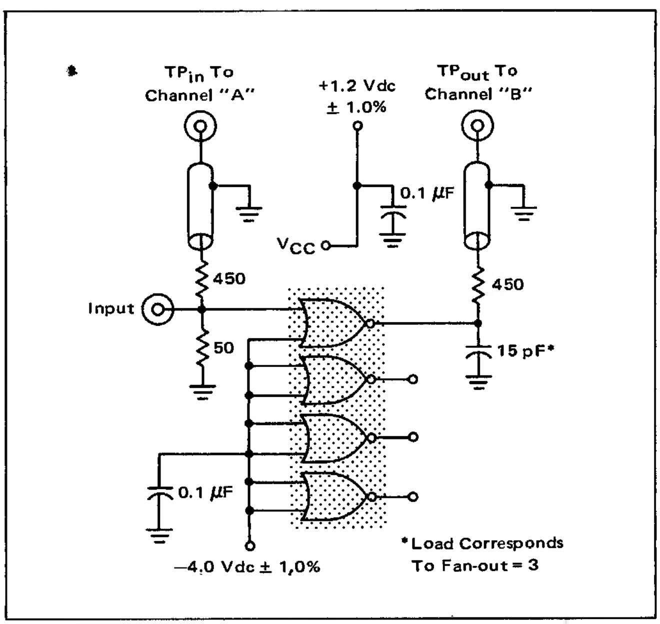
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs without pull-down resistors are tested with a 1.5 kΩ resistor to V_{EE}.

Characteristic	Symbol	Pin Under Test	MC1210-1212 Test Limits							MC1010-1012 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7														
MC1210/MC1010		↓	-	-	-	32	-	-	mAdc	-	-	-	32	-	-	mAdc
MC1211/MC1011		↓	-	-	-	26	-	-	↓	-	-	-	26	-	-	↓
MC1212/MC1012		↓	-	-	-	18	-	-	↓	-	-	-	18	-	-	↓
Input Current	I_{in}	1	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		2	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	3	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		3	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	3	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		3	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{1+3-}	3	4.0	7.5	4.5	7.5	6.0	9.0	ns	4.0	7.5	4.5	7.5	5.5	8.5	ns
	t_{1-3+}	↓	5.0	7.0	5.0	7.0	6.0	9.0	↓	5.0	7.0	5.0	7.0	5.5	8.0	↓
(Fan-Out = 15)	t_{1+3-}	↓	18	-	18	-	22	-	↓	18	-	18	-	20	-	↓
	t_{1-3+}	↓	6.0	-	6.0	-	9.0	-	↓	6.0	-	6.0	-	7.0	-	↓
Rise Time (Fan-Out = 3)	t_{3+}	↓	4.0	7.5	4.0	7.0	5.0	8.0	↓	4.0	7.0	4.0	7.0	4.5	7.5	↓
Fall Time (Fan-Out = 3)	t_{3-}	↓	6.0	8.5	6.0	8.0	7.0	10	↓	6.0	8.0	6.0	8.0	6.5	9.0	↓

* Individually test each input using the pin connections shown.
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

SWITCHING TIME TEST CIRCUIT @ 25°C

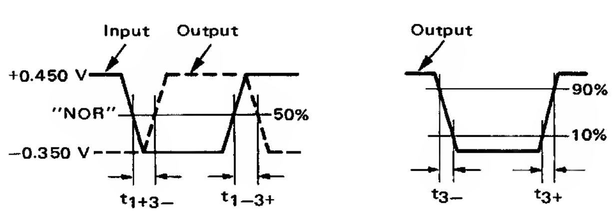


	@Test Temperature	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L
		TEST VOLTAGE/CURRENT VALUES				
		Vdc ±1.0%				mAdc
MC1210-1212	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1010-1012	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Characteristic	Symbol	Pin Under Test	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7						
MC1210/MC1010		↓	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14
MC1211/MC1011		↓	-	-	-	↓	-	↓
MC1212/MC1012		↓	-	-	-	↓	-	↓
Input Current	I_{in}	1	-	-	1	2, 4, 5, 7, 9, 10, 12, 13	-	14
		2	-	-	2	1, 4, 5, 7, 9, 10, 12, 13	-	14
Input Leakage Current	I_R	Inputs*	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	3	1	-	-	2, 4, 5, 7, 9, 10, 12, 13	3	14
		3	2	-	-	1, 4, 5, 7, 9, 10, 12, 13	3	14
"NOR" Logical "0" Output Voltage	V_{OL}	3	-	1	-	2, 4, 5, 7, 9, 10, 12, 13	-	14
		3	-	2	-	1, 4, 5, 7, 9, 10, 12, 13	-	14
Switching Times			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2V)
Propagation Delay (Fan-Out = 3)	t_{1+3-}	3	1	3	-	2, 4, 5, 7, 9, 10, 12, 13	-	14
	t_{1-3+}	↓	↓	↓	-	↓	-	↓
(Fan-Out = 15)	t_{1+3-}	↓	↓	↓	-	↓	-	↓
	t_{1-3+}	↓	↓	↓	-	↓	-	↓
Rise Time (Fan-Out = 3)	t_{3+}	↓	↓	↓	-	↓	-	↓
Fall Time (Fan-Out = 3)	t_{3-}	↓	↓	↓	-	↓	-	↓

PROPAGATION DELAY RISE AND FALL TIMES



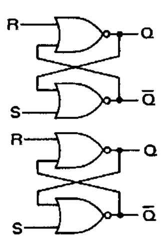
Input Pulse t_r and t_f = 5.0 ± 0.5 ns

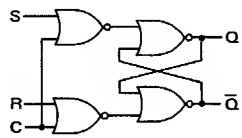
Switching waveforms shown for pulse in on pin 1 and pulse out on pin 3, however all other Input-output combinations will meet the limits specified.

SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

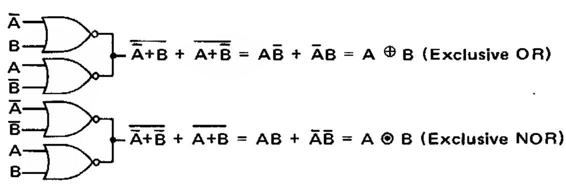
The MC1010-1012/MC1210-1212 quad 2-input NOR gates are very useful in building more complex functions. For example, two R-S flip-flops may be obtained by cross-coupling gates, or a single gated R-S flip-flop may be obtained (see diagram below). Dual clocked R-S flip-flops are available in MECL II (see flip-flop section). The quad 2-input gate may also be used as a dual exclusive OR or NOR by ORing the outputs as shown below.





C is the gating input. Low level allows new data to be set into the flip-flop.

FIGURE 1 - FLIP-FLOPS OBTAINED BY USING MC1010-1012/MC1210-1212 GATES



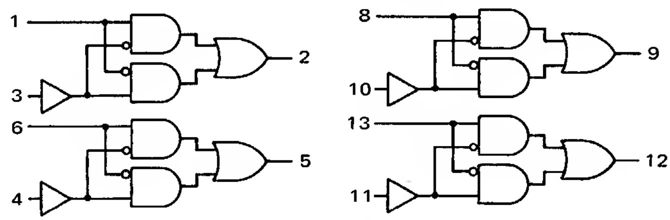
The nominal propagation delay through the Exclusive OR or NOR is 4.0 ns. The Exclusive NORs or ORs are often used as comparator gates giving an output whenever the input data is the same or different. Parity checkers are also built from Exclusive OR gates.

FIGURE 2 - DUAL EXCLUSIVE "OR" or "NOR" GATES

MC1030
MC1230

Four gate arrays designed to provide four Exclusive OR functions. The output is high if and only if one input is high and all other inputs are low.

POSITIVE LOGIC



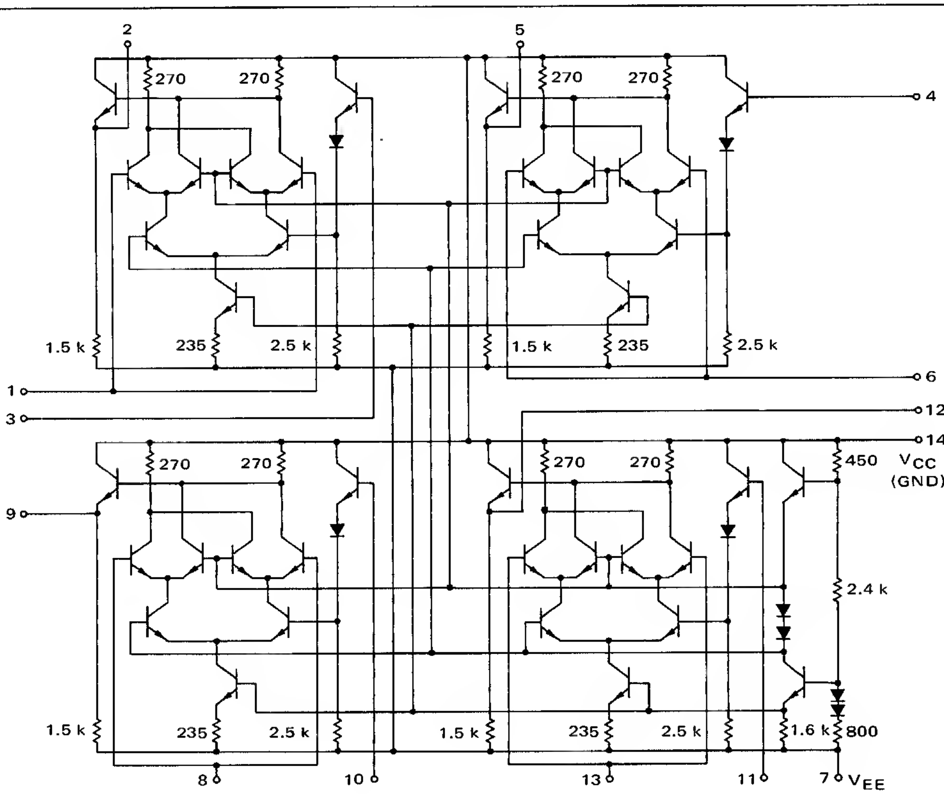
$2 = 1 \bullet \overline{3} + \overline{1} \bullet 3$

DC Input Loading Factor: Pins 1, 6, 8, 13 = 1.5
Pins 3, 4, 10, 11 = 1

DC Output Loading Factor = 25

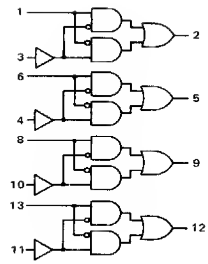
Power Dissipation = 130 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal

MC1030, MC1230 (continued)



ELECTRICAL CHARACTERISTICS

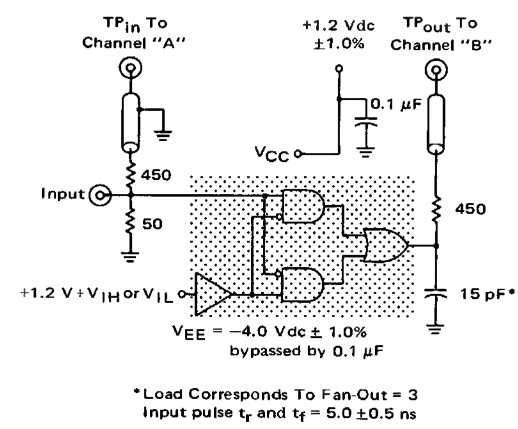
Test procedures are shown for only one gate. The other gates are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1230 Test Limits							MC1030 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7	-	--	-	33	-	-	mAdc	-	-	-	33	-	-	mAdc
Input Current	I_{in}	1 3	- -	- -	- -	150 100	- —	- -	µAdc µAdc	- -	- -	- -	150 100	- -	- -	µAdc µAdc
Input Leakage Current	I_R	1 3	- -	- -	- -	0.4 0.2	- -	2.0 1.0	µAdc µAdc	- -	- -	- -	0.4 0.2	- -	2.0 1.0	µAdc µAdc
Logical "1" Output Voltage	V_{OH} ‡	2 2	-0.990 -0.990	-0.825 -0.825	-0.850 -0.850	-0.700 -0.700	-0.700 -0.700	-0.530 -0.530	Vdc Vdc	-0.895 -0.895	-0.740 -0.740	-0.850 -0.850	-0.700 -0.700	-0.775 -0.775	-0.615 -0.615	Vdc Vdc
Logical "0" Output Voltage	V_{OL}	2 2	-1.890 -1.890	-1.580 -1.580	-1.800 -1.800	-1.500 -1.500	-1.720 -1.720	-1.380 -1.380	Vdc Vdc	-1.830 -1.830	-1.525 -1.525	-1.800 -1.800	-1.500 -1.500	-1.760 -1.760	-1.435 -1.435	Vdc Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{1+2-}	2	5.0	8.5	5.0	8.5	6.0	10	ns	5.0	8.5	5.0	8.5	6.0	9.0	ns
	t_{1-2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{1+2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{1-2-}		6.0	9.0	6.0	9.0		10		6.0	9.0	6.0	9.0	6.0	9.5	
	t_{3+2-}		5.0	8.5	5.0	8.5		10		5.0	8.5	5.0	8.5	6.0	9.0	
	t_{3-2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{3+2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{3-2-}		6.0	9.0	6.0	9.0		10		6.0	9.0	6.0	9.0	6.0	9.5	
Rise Time	t_{2+}		5.0	8.5	5.0	8.5		9.5		5.0	8.5	5.0	8.5	6.0	9.0	
	t_{2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
Fall Time	t_{2-}			8.5		8.5		10			8.5		8.5	6.0	9.0	
	t_{2-}		6.0	9.0	6.0	9.0		10		6.0	9.0	6.0	9.0	6.0	9.5	

‡V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

*V_{IL} or V_{IH} value as given plus +1.2 V

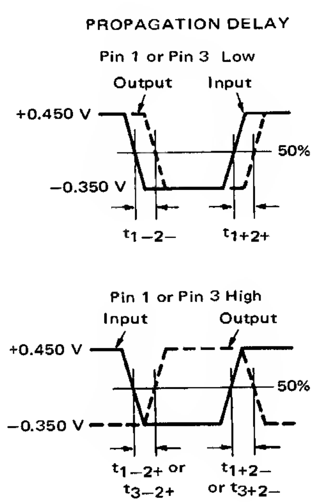
SWITCHING TIME TEST CIRCUIT @ 25°C

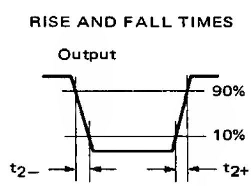


@Test Temperature		V_{IL}	V_{IH}	$V_{IH\,max}$	V_{EE}	I_L
		TEST VOLTAGE/CURRENT VALUES				
		Vdc ±1.0%				mAdc
MC1230	−55°C	-1.580	-0.990	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+125°C	-1.380	-0.700	-	-5.2	-2.5
MC1030	0°C	-1.525	-0.895	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+75°C	-1.435	-0.775	-	-5.2	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Characteristic	Symbol	Pin Under Test	V_{IL}	V_{IH}	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	1, 3, 4, 6, 7, 8, 10, 11, 13	-	14
Input Current	I_{in}	1	-	-	1	3, 7	-	14
		3	-	-	3	1, 7	-	14
Input Leakage Current	I_R	1	-	-	-	1, 3, 7	-	14
		3	-	-	-	1, 3, 7	-	14
Logical "1" Output Voltage	V_{OH} ‡	2	1	3	-	7	2	14
		2	3	1	-	7	2	14
Logical "0" Output Voltage	V_{OL}	2	1, 3	-	-	7	-	14
		2	-	1, 3	-	7	-	14
Switching Times (Fan-Out = 3)			V_{IL}*	V_{IH}*	Pulse In	V_{EE} = −4.0 Vdc	Pulse Out	(+1.2 Vdc)
Propagation Delay	t_{1+2-}	2	-	3	1	7	2	14
	t_{1-2+}		-	3				
	t_{1+2+}		3	-				
	t_{1-2-}		3	-				
	t_{3+2-}		-	1	3			
	t_{3-2+}		-	1				
	t_{3+2+}		1	-				
	t_{3-2-}		1	-				
Rise Time	t_{2+}		-	3	1			
	t_{2+}		1	-	3			
Fall Time	t_{2-}		-	3	1			
	t_{2-}		1	-	3			





Switching waveforms shown for pulse in on pin 1 or pin 3 and pulse out on pin 2, however all other input-output combinations will meet the limits specified.

SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

SAMPLE TRUTH TABLE

	Inputs		Output
Pin No.	1	3	2
	0	0	0
	0	1	1
	1	0	1
	0	0	0

The Exclusive OR may be symbolized as:

The MC1030/MC1230 quad Exclusive OR gate is a high-speed device employing the series gating technique. The quad Exclusive OR (⊕) is useful in many applications such as data comparison, parity generation and checking, frequency mixing, decision circuitry, and code conversion circuitry. The output of each Exclusive OR is high if the two inputs are at different logic levels, while it is low if the inputs are at the same level.

Figure 1 illustrates the comparison of two 8-bit words. The OR output goes high if any Source "A" bit is not the same as the corresponding Source "B" bit. The comparison of two 16-bit words is possible by using two more MC1030/MC1230's, the other half of the MC1004/MC1204, and ORing the two OR outputs together. Note that the MC1030/MC1230 gates are paired together (in Wired-OR configuration) to save extra inputs on the MC1004/MC1204. Typical propagation delay time from inputs to the output of the MC1004/MC1204 is 10 ns.

Figure 2 illustrates checking the bits of a word for odd parity; if the sum of the inputs is odd, the output will be high. (It is also possible to mix MC1030/MC1230 quad Exclusive OR gates and MC1031/MC1231 quad Exclusive NOR gates to obtain the same function.)

FIGURE 1 – DATA COMPARATOR

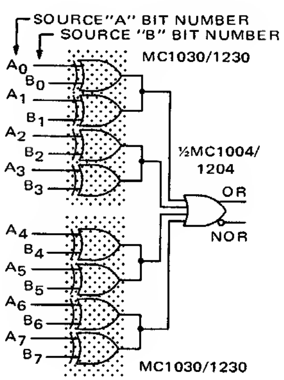
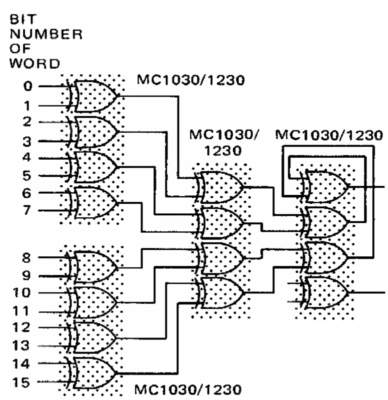


FIGURE 2 – 25 ns 16-BIT PARITY CHECKER (Odd Parity)

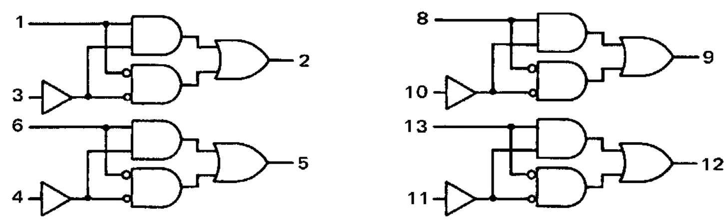


QUAD EXCLUSIVE "NOR" GATES

MC1031
MC1231

Four gate arrays designed to provide four Exclusive NOR functions. The output is high if and only if the two inputs are at the same logic level.

POSITIVE LOGIC



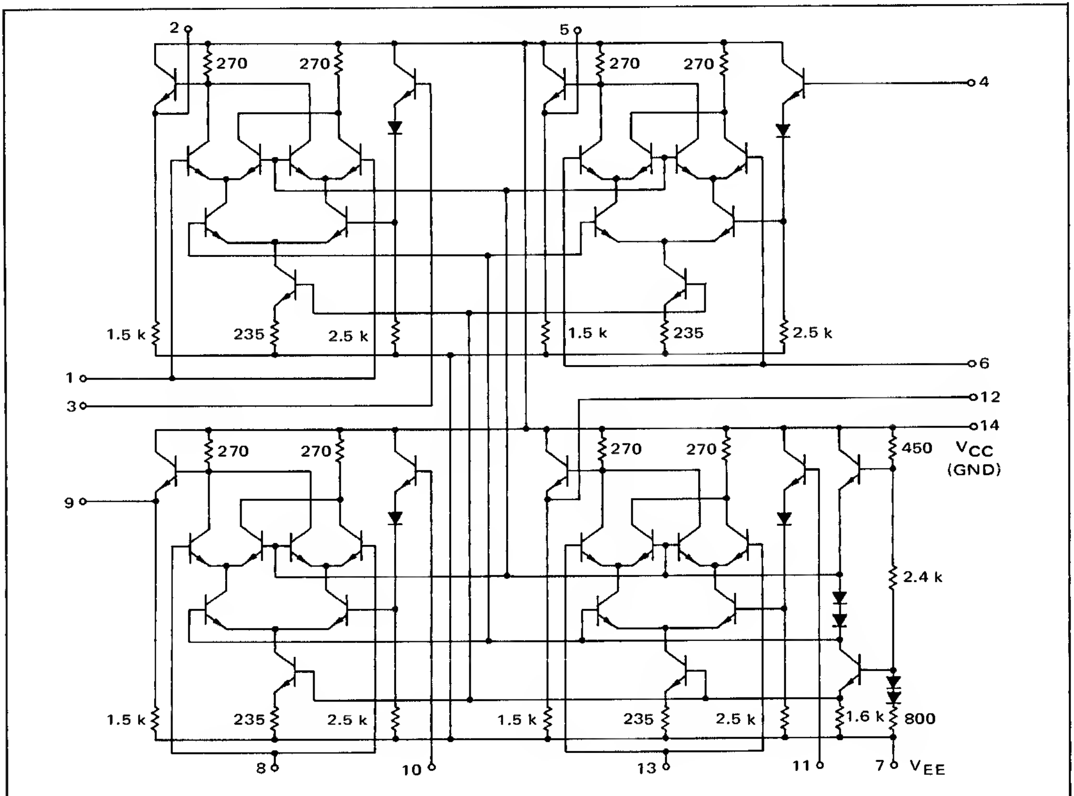
$2 = 1 \bullet 3 + \overline{1} \bullet \overline{3}$

DC Input Loading Factor: Pins 1, 6, 8, 13 = 1.5
Pins 3, 4, 10, 11 = 1

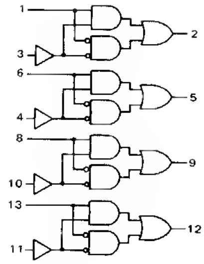
DC Output Loading Factor = 25

Power Dissipation = 130 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal



ELECTRICAL CHARACTERISTICS

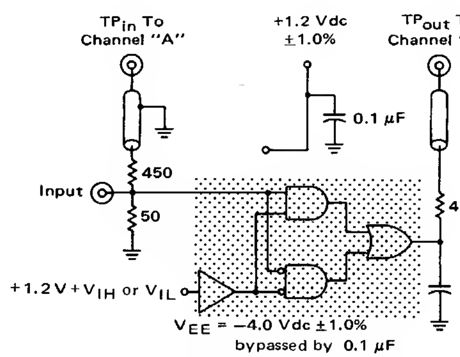
Test procedures are shown for only one gate. The other gates are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1231 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1031 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	--	-	33	-	-	mAdc	-	-	-	33	-	-	mAdc
Input Current	I_{in}	1 3	- -	- -	- -	150 100	- —	- -	μAdc μAdc	- -	- -	- -	150 100	- -	- -	μAdc μAdc
Input Leakage Current	I_R	1 3	- -	- -	- -	0.4 0.2	- -	2.0 1.0	μAdc μAdc	- -	- -	- -	0.4 0.2	- -	2.0 1.0	μAdc μAdc
Logical "1" Output Voltage	V_{OH} ‡	2 2	-0.990 -0.990	-0.825 -0.825	-0.850 -0.850	-0.700 -0.700	-0.700 -0.700	-0.530 -0.530	Vdc Vdc	-0.895 -0.895	-0.740 -0.740	-0.850 -0.850	-0.700 -0.700	-0.775 -0.775	-0.615 -0.615	Vdc Vdc
Logical "0" Output Voltage	V_{OL}	2 2	-1.890 -1.890	-1.580 -1.580	-1.800 -1.800	-1.500 -1.500	-1.720 -1.720	-1.380 -1.380	Vdc Vdc	-1.830 -1.830	-1.525 -1.525	-1.800 -1.800	-1.500 -1.500	-1.760 -1.760	-1.435 -1.435	Vdc Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{1+2-}	2	5.0	8.5	5.0	8.5	6.0	10	ns	5.0	8.5	5.0	8.5	6.0	9.0	ns
	t_{1-2+}	↓	↓	8.0	↓	8.0	↓	9.0	↓	↓	8.0	↓	8.0	5.0	8.5	↓
	t_{1+2+}	↓	↓	8.0	↓	8.0	↓	9.0	↓	↓	8.0	↓	8.0	5.0	8.5	↓
	t_{1-2-}	↓	6.0	9.0	6.0	9.0	↓	10	↓	6.0	9.0	6.0	9.0	6.0	9.5	↓
	t_{3+2-}	↓	5.0	8.5	5.0	8.5	↓	10	↓	5.0	8.5	5.0	8.5	6.0	9.0	↓
	t_{3-2+}	↓	↓	8.0	↓	8.0	↓	9.0	↓	↓	8.0	↓	8.0	5.0	8.5	↓
	t_{3+2+}	↓	↓	8.0	↓	8.0	↓	9.0	↓	↓	8.0	↓	8.0	5.0	8.5	↓
	t_{3-2-}	↓	6.0	9.0	6.0	9.0	↓	10	↓	6.0	9.0	6.0	9.0	6.0	9.5	↓
Rise Time	t_{2+}	↓	5.0	8.5	5.0	8.5	↓	9.5	↓	5.0	8.5	5.0	8.5	6.0	9.0	↓
	t_{2+}	↓	↓	8.0	↓	8.0	↓	9.0	↓	↓	8.0	↓	8.0	5.0	8.5	↓
Fall Time	t_{2-}	↓	↓	8.5	↓	8.5	↓	10	↓	↓	8.5	↓	8.5	6.0	9.0	↓
	t_{2-}	↓	6.0	9.0	6.0	9.0	↓	10	↓	6.0	9.0	6.0	9.0	6.0	9.5	↓

‡V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

*V_{IL} or V_{IH} value as given plus +1.2 V

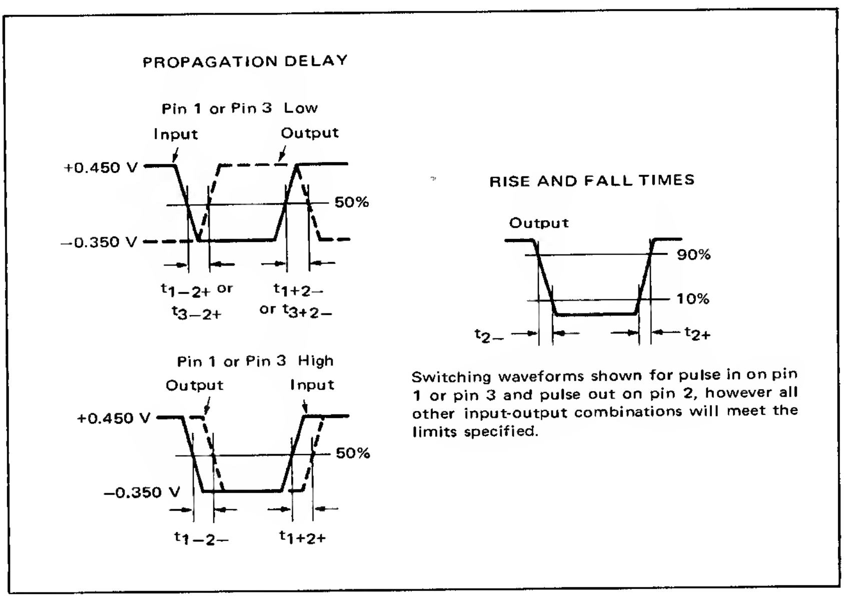
SWITCHING TIME TEST CIRCUIT @ 25°C



*Load Corresponds To Fan-Out = 3
Input pulse t_r and t_f = 5.0 ±0.5 ns

@Test Temperature		V_{IL}	V_{IH}	$V_{IH\,max}$	V_{EE}	I_L
		TEST VOLTAGE/CURRENT VALUES				
		Vdc ±1.0%				mAdc
MC1231	−55°C	-1.580	-0.990	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+125°C	-1.380	-0.700	-	-5.2	-2.5
MC1031	0°C	-1.525	-0.895	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+75°C	-1.435	-0.775	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	V_{IL}	V_{IH}	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
			TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					
Power Supply Drain Current	I_E	7	-	-	-	1, 3, 4, 6, 7, 8, 10, 11, 13	-	14
Input Current	I_{in}	1	-	-	1	3, 7	-	14
		3	-	-	3	1, 7	-	14
Input Leakage Current	I_R	1	-	-	-	1, 3, 7	-	14
		3	-	-	-	1, 3, 7	-	14
Logical "1" Output Voltage	V_{OH} ‡	2	1, 3	-	-	7	2	14
		2	-	1, 3	-	7	2	14
Logical "0" Output Voltage	V_{OL}	2	1	3	-	7	-	14
		2	3	1	-	7	-	14
Switching Times (Fan-Out = 3)			V_{IL}*	V_{IH}*	Pulse In	V_{EE} = −4.0 Vdc	Pulse Out	(+1.2 Vdc)
Propagation Delay	t_{1+2-}	2	3	-	1	7	2	14
	t_{1-2+}		3	-				
	t_{1+2+}		-	3				
	t_{1-2-}		-	3				
	t_{3+2-}		1	-	3			
	t_{3-2+}		1	-				
	t_{3+2+}		-	1				
	t_{3-2-}		-	1				
Rise Time	t_{2+}		3	-	1			
	t_{2+}		-	1	3			
Fall Time	t_{2-}		3	-	1			
	t_{2-}		-	1	3			



Switching waveforms shown for pulse in on pin 1 or pin 3 and pulse out on pin 2, however all other input-output combinations will meet the limits specified.

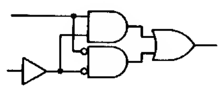
SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

SAMPLE TRUTH TABLE

	Inputs		Output
Pin No.	1	3	2
	0	0	1
	0	1	0
	1	0	0
	1	1	1

The Exclusive NOR may be symbolized as:



or

The MC1031/MC1231 quad Exclusive NOR gate is obtained by changing circuit interconnections of the MC1030/MC1230 through use of a different metal mask. The quad Exclusive NOR (⊙) is useful for data comparison, parity generation and checking, decision circuitry, code conversion circuitry, and frequency mixing. The output of each Exclusive NOR is high if the two inputs are at the same logic levels. The Exclusive NOR is the logical complement or inversion of the Exclusive OR.

Figure 1 illustrates a controlled data inverter in which parallel data can be either inverted or not inverted with a single control level. For example, the input information is passed directly to the output if C is at a high level. Exclusive OR gates may also be used to perform this function. The C input would be inverted for the same logic function.

Figure 2 illustrates checking the bits of a word for even parity; if the sum of the inputs is even, the output will be high. (It is also possible to mix MC1031/MC1231 quad Exclusive NOR gates and MC1030/MC1230 quad Exclusive OR gates to obtain the same function.)

FIGURE 1 – CONTROLLED DATA INVERTER

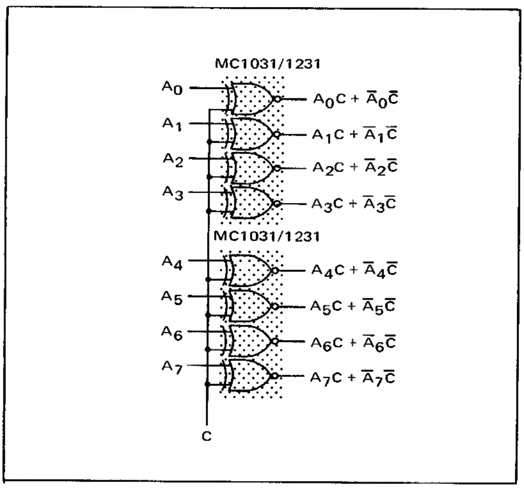
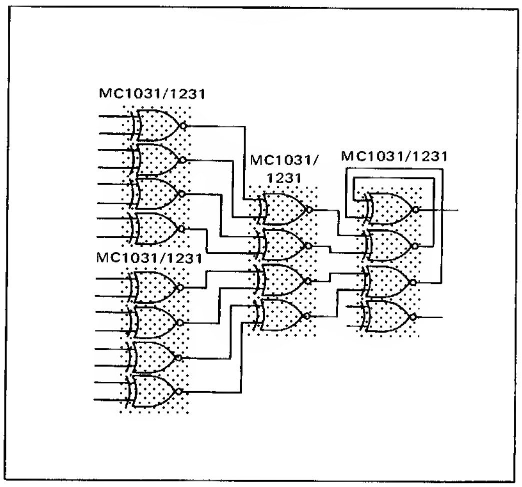


FIGURE 2 – 25 ns 16-BIT PARITY CHECKER (Even Parity)

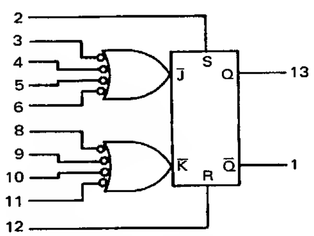


85-MHz AC-COUPLED
J-K FLIP-FLOPS

MC1013
MC1213

Designed for use at clock frequencies to 70 MHz minimum (85 MHz typical). Logic performing inputs ($\bar{J}$ and $\bar{K}$) are available, as well as dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 125 mW typical

*Any $\bar{J}$ or $\bar{K}$ input, not used for $\bar{C}_D$.
**$\bar{C}_D$ obtained by connecting one $\bar{J}$ and one $\bar{K}$ input together.

The $\bar{J}$ and $\bar{K}$ inputs refer to logic levels while the $\bar{C}_D$ input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to a logical "1" only while the $\bar{C}_D$ input is in a logic "1" state. ($\bar{C}_D$ maximum "1" level = V_{CC} −0.6 V). Clock $\bar{C}_D$ is obtained by tying one $\bar{J}$ and one $\bar{K}$ input together.

R-S TRUTH TABLE

	R	S	Q^{n+1}
Pin No.	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\bar{J}$·$\bar{K}$ Inputs Are Static

$\bar{J}_D$·$\bar{K}_D$ TRUTH TABLE

	$\bar{J}_D$	$\bar{K}_D$	Q^{n+1}
Pin No.	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\bar{Q}^n$

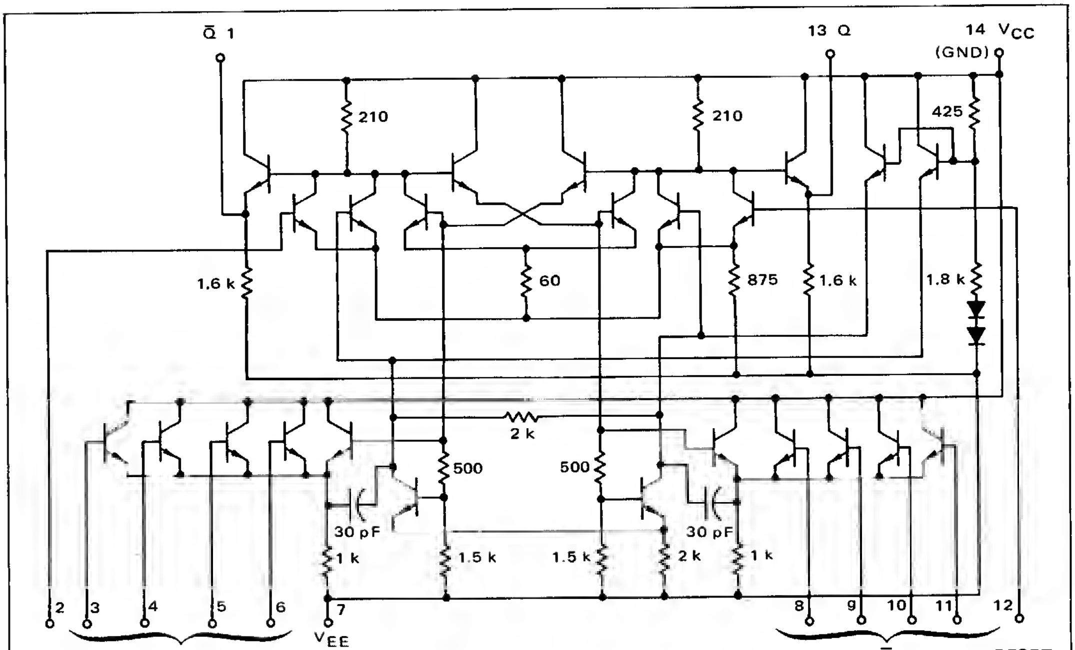
All Other $\bar{J}$-$\bar{K}$ Inputs And The R-S Inputs Are At a "0" Level

CLOCKED $\bar{J}$·$\bar{K}$ TRUTH TABLE

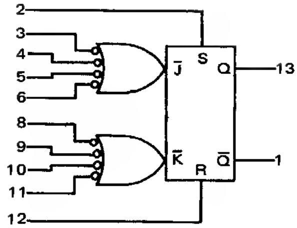
	$\bar{J}$	$\bar{K}$	$\bar{C}_D$	Q^n
Pin No.	*	*	**	13
	ϕ	ϕ	0	Q^n
	0	0	1	$\bar{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All Other $\bar{J}$-$\bar{K}$ Inputs And The R-S Inputs Are At a "0" Level

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1213 Test Limits							MC1013 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	29	-	-	mAdc	-	-	-	29	-	-	mAdc
Input Current	I_{in}	2	-	-	-	100	-	-	µAdc	-	-	-	100	-	-	µAdc
		3	-	-	-		-	-		-	-	-		-	-	
		4	-	-	-		-	-		-	-	-		-	-	
		5	-	-	-		-	-		-	-	-		-	-	
		6	-	-	-		-	-		-	-	-		-	-	
		8	-	-	-		-	-		-	-	-		-	-	
		9	-	-	-		-	-		-	-	-		-	-	
		10	-	-	-		-	-		-	-	-		-	-	
		11	-	-	-		-	-		-	-	-		-	-	
		12	-	-	-		-	-		-	-	-		-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	µAdc	-	-	-	0.2	-	1.0	µAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	13	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	13	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q̄" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q̄" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q" or "Q̄" Latch Voltage	V_L	2	-1.16	-1.34	-1.09	-1.21	-0.93	-1.07	Vdc	-1.11	-1.25	-1.09	-1.21	-1.02	-1.14	Vdc
		12	-1.16	-1.34	-1.09	-1.21	-0.93	-1.07	Vdc	-1.11	-1.25	-1.09	-1.21	-1.02	-1.14	Vdc
Input Toggle Frequency (See Figures 3 & 4)	f_{Tog}	13	-	-	70	-	-	-	MHz	-	-	70	-	-	-	MHz
Sensitivity (No Toggle)	-	1			See Figure 1							See Figure 1				
		13			See Figure 1							See Figure 1				
Sensitivity (Toggle)	-	1, 13			See Figure 2							See Figure 2				
Switching Times ④			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{6+1+}	1	6.0	8.5	6.0	8.5	8.0	10.5	ns	6.0	8.5	6.0	8.5	6.5	9.0	ns
	t_{6+1-}	1					7.5									
	t_{8+13+}	13					8.0									
	t_{8+13-}	13					7.5									
Rise Time	t_{1+}	1	4.0	7.5	4.0	7.5	5.5	9.5		4.0	7.5	4.0	7.5	5.0	8.0	
	t_{13+}	13	4.0		4.0		5.5	9.5		4.0		4.0			8.0	
Fall Time	t_{1-}	1	5.0		5.0		7.5	10		5.0		5.0			8.5	
	t_{13-}	13	5.0		5.0		7.5	10		5.0		5.0			8.5	

* Individually test each input using the pin connections shown.
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).
① $V_{in(set)} = V_{OH}$ then $V_{OL(max)}$.
② $V_{in(reset)} = V_{OH}$ then $V_{OL(max)}$.
③ Input voltage is adjusted to obtain $dV_{"1"}/dV_{in} = \infty$.
④ AC fan-out = 3

	@Test Temperature	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L
		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0%				mAdc
MC1213	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1013	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Characteristic	Symbol	Pin Under Test	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	dV_{in}	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
Input Current	I_{in}	2	-	-	2	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
		3	-	-	3	2, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	
		4	-	-	4	2, 3, 5, 6, 7, 8, 9, 10, 11, 12	-	-	
		5	-	-	5	2, 3, 4, 6, 7, 8, 9, 10, 11, 12	-	-	
		6	-	-	6	2, 3, 4, 5, 7, 8, 9, 10, 11, 12	-	-	
		8	-	-	8	2, 3, 4, 5, 6, 7, 9, 10, 11, 12	-	-	
		9	-	-	9	2, 3, 4, 5, 6, 7, 8, 10, 11, 12	-	-	
		10	-	-	10	2, 3, 4, 5, 6, 7, 8, 9, 11, 12	-	-	
		11	-	-	11	2, 3, 4, 5, 6, 7, 8, 9, 10, 12	-	-	
		12	-	-	12	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	13	-	-	2 ①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	13	-	14
"Q" Logical "0" Output Voltage	V_{OL}	13	-	-	12 ②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	-	-	14
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-	-	12 ②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1	-	14
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	-	-	2 ①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
"Q" or "$\bar{Q}$" Latch Voltage	V_L	2	-	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11	-	2 ③	14
		12	-	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11	-	12 ③	14
			Pulse In	Pulse Out		$V_{EE} = -4.0$ Vdc			(+1.2V)
Input Toggle Frequency (See Figures 3 & 4)	f_{Tog}	13	6, 8	13	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	-	14
Sensitivity (No Toggle)	-	1	6, 8	1	-		-	-	
		13	6, 8	13	-		-	-	
Sensitivity (Toggle)	-	1, 13	6, 8	1, 13	-		-	-	
Switching Times ④									
Propagation Delay	t_{6+1+}	1	6	1	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	-	14
	t_{6+1-}	1	6	1	-		-	-	
	t_{8+13+}	13	8	13	-		-	-	
	t_{8+13-}	13	8	13	-		-	-	
Rise Time	t_{1+}	1	6	1	-		-	-	
	t_{13+}	13	8	13	-		-	-	
Fall Time	t_{1-}	1	6	1	-		-	-	
	t_{13-}	13	8	13	-		-	-	

FIGURE 1 - SENSITIVITY (NO TOGGLE)

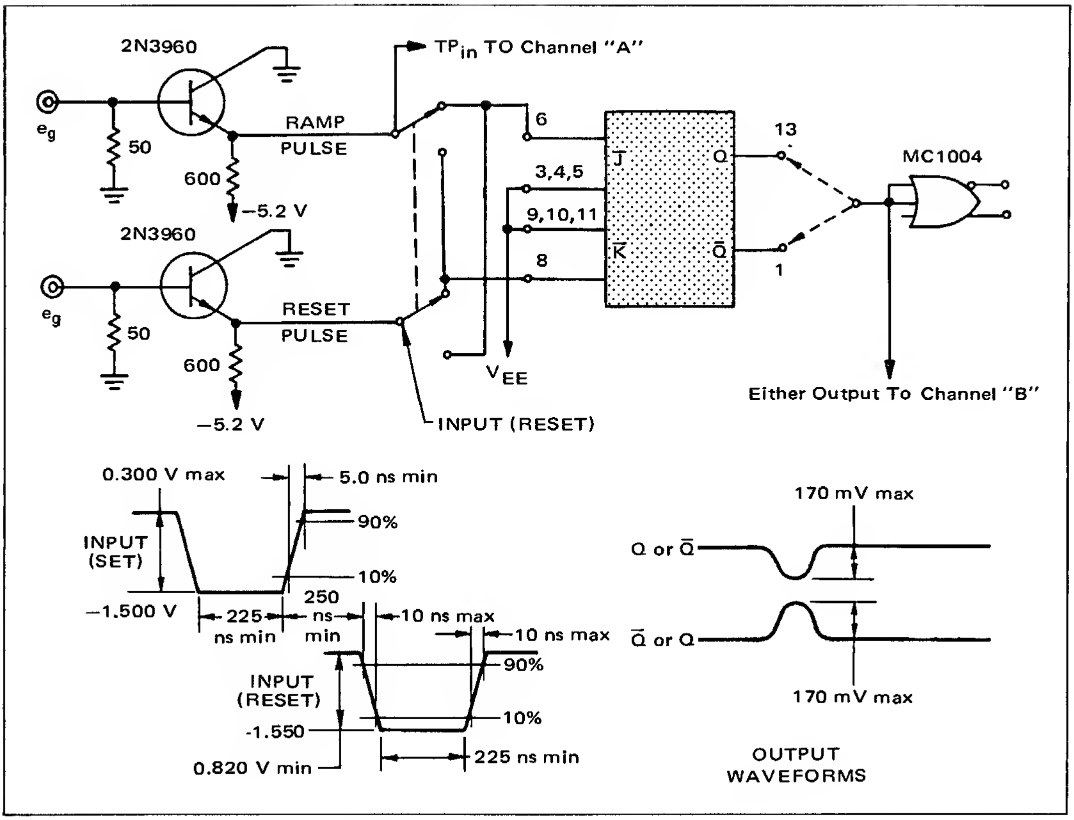
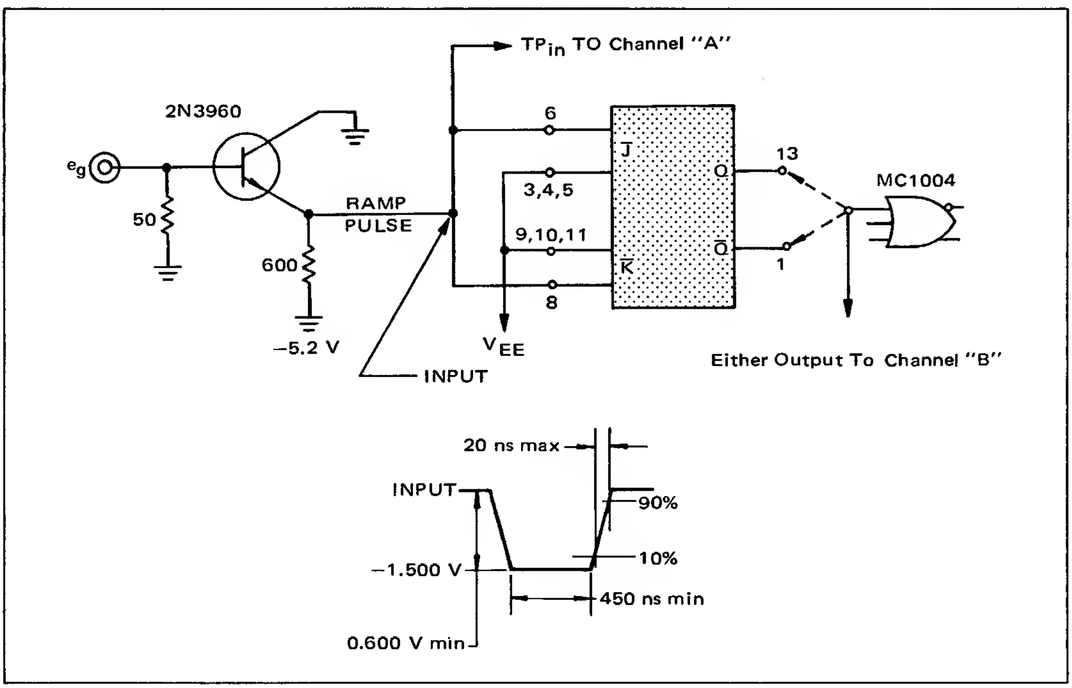


FIGURE 2 - SENSITIVITY (TOGGLE)



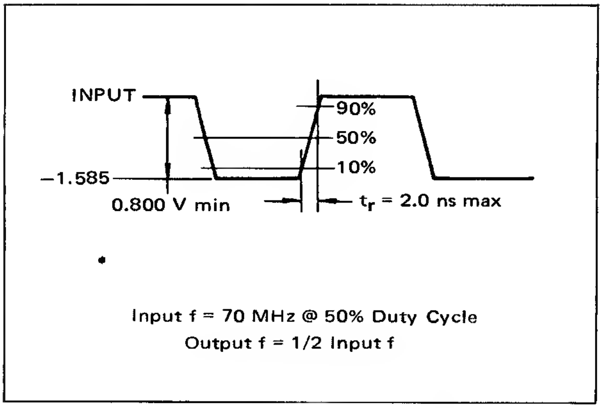
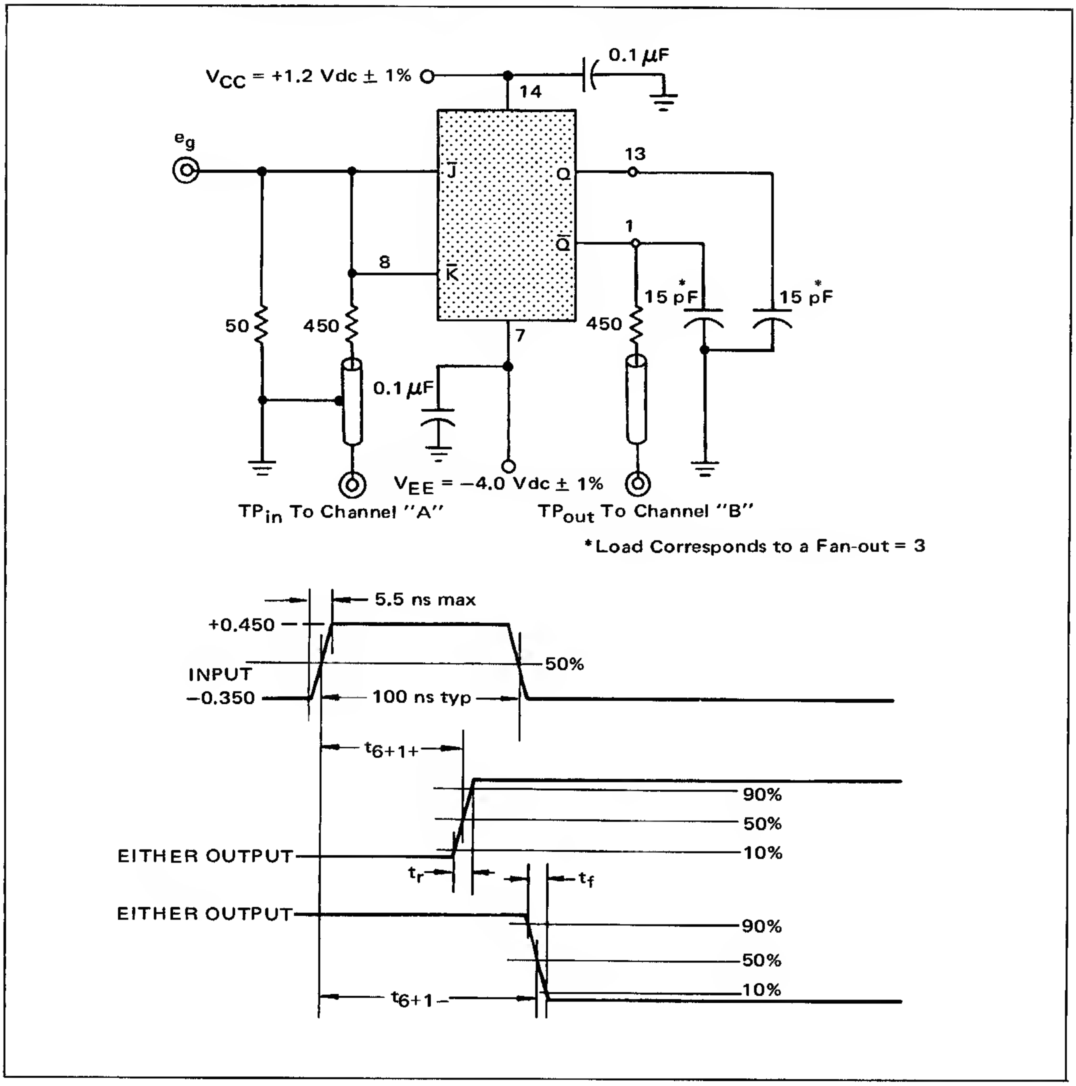


FIGURE 3 - INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

FIGURE 4 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



APPLICATIONS INFORMATION

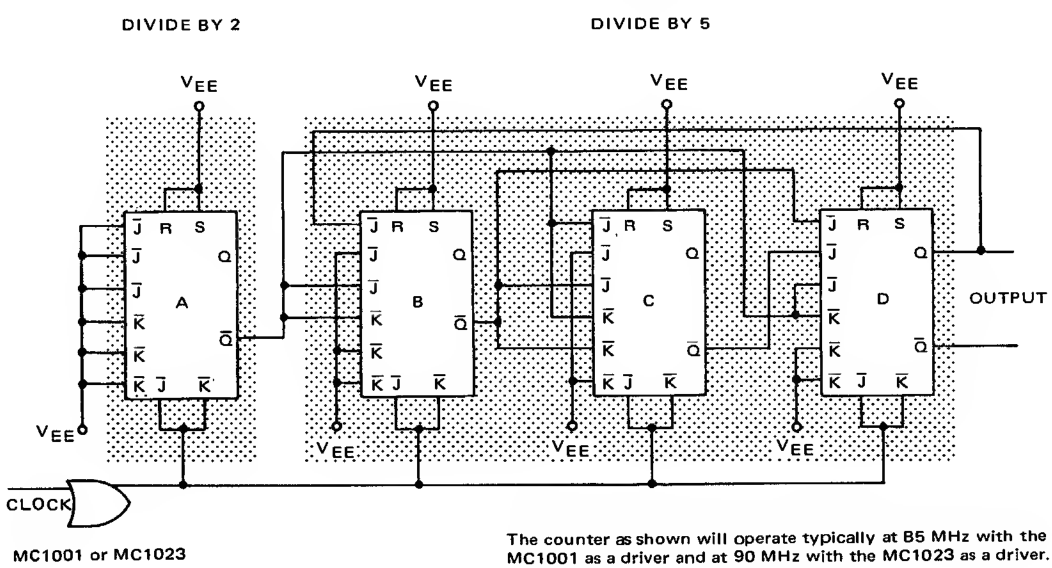
The MC1013/MC1213 J-K flip-flop is used in both counter and shift register applications. Typically the flip-flop will shift and toggle at 85 MHz. Flip-flop operation is illustrated by the curves shown on page 2-125. For a complete characterization of the device, refer to Application Note AN-280. Circuit operation is essentially the same as the MC314/MC364 flip-flop which is explained in Application Note AN-244. Due to the four $\bar{J}$ and four $\bar{K}$ inputs, many clocked and ripple through counters may be built without additional logic. Figure 5 is a table illustrating the $\bar{J}$ and $\bar{K}$ input equations for clocked counters, divide by 3 through 10. Figure 6 is a clocked BCD counter utilizing the logic equations shown in the table.

FIGURE 5 - INPUT EQUATIONS FOR CLOCKED COUNTERS

Divide By:	$\bar{J}_A$	$\bar{K}_A$	$\bar{J}_B$	$\bar{K}_B$	$\bar{J}_C$	$\bar{K}_C$	$\bar{J}_D$	$\bar{K}_D$
3	B	0	$\bar{A}$	0	--	--	--	--
4	0	0	$\bar{A}$	$\bar{A}$	--	--	--	--
5	C	0	$\bar{A}$	$\bar{A}$	$\bar{A}+\bar{B}$	0	--	--
6	0	0	$\bar{A}+C$	$\bar{A}$	$\bar{A}+\bar{B}$	$\bar{A}$	--	--
7	BC	0	$\bar{A}$	$\overline{A+C}$	$\bar{A}+\bar{B}$	$\bar{B}$	--	--
8	0	0	$\bar{A}$	$\bar{A}$	$\bar{A}+\bar{B}$	$\bar{A}+\bar{B}$	--	--
9	D	0	$\bar{A}$	$\bar{A}$	$\bar{A}+\bar{B}$	$\bar{A}+\bar{B}$	$\bar{A}+\bar{B}+\bar{C}$	0
10	0	0	$\bar{A}+D$	$\bar{A}$	$\bar{A}+\bar{B}$	$\bar{A}+\bar{B}$	$\bar{A}+\bar{B}+\bar{C}$	$\bar{A}$

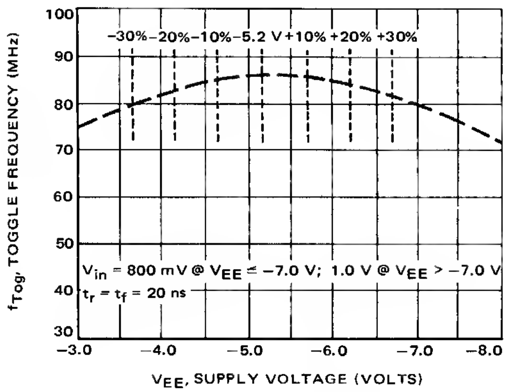
0 (logic zero) $\leqslant -1.6$ V (pin usually tied to V_{EE}).
All but $\div$ 7 may be obtained without additional gating.
All $\bar{J}$ inputs and all $\bar{K}$ inputs are ORed together.

FIGURE 6 - CLOCKED BCD COUNTER USING MECL $\bar{J}$-$\bar{K}$ FLIP-FLOPS



The counter as shown will operate typically at 85 MHz with the MC1001 as a driver and at 90 MHz with the MC1023 as a driver.

FIGURE 7 - TYPICAL TOGGLE FREQUENCY versus V_{EE}



ALL UNUSED INPUTS RETURNED TO V_{EE}.
V_{EE} = −5.2 V, V_{in} = 800 mV, T_A = 25°C unless otherwise noted.
——— WORST CASE – – – –TYPICAL

FIGURE 8 - TYPICAL AND WORST CASE TOGGLE FREQUENCY versus AMBIENT TEMPERATURE

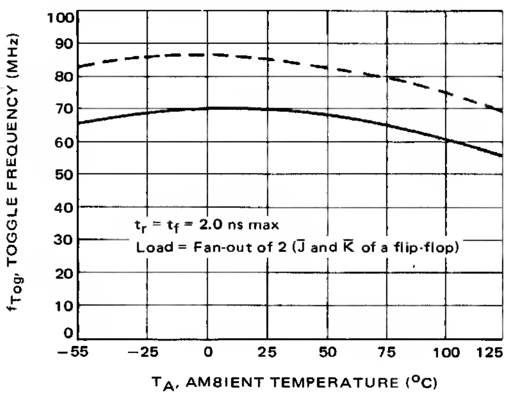


FIGURE 10 - TIME TO DOMINATE

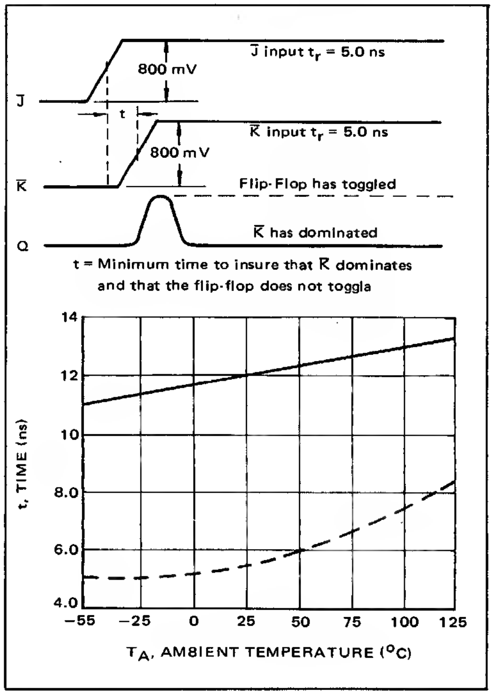


FIGURE 9 - AMPLITUDE versus RISE TIME TO INSURE TOGGLE

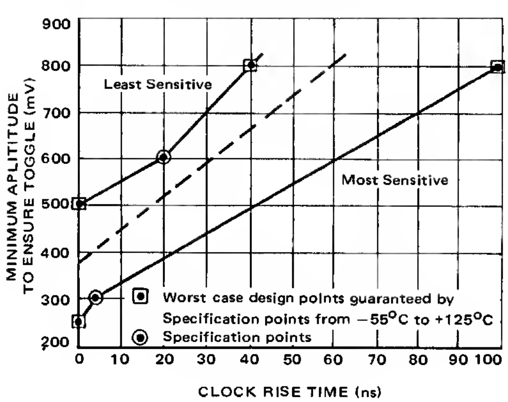
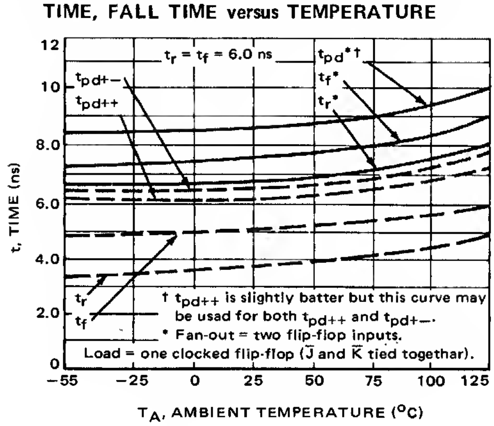


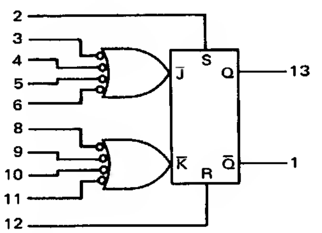
FIGURE 11 - PROPAGATION DELAY TIMES, RISE TIME, FALL TIME versus TEMPERATURE



MC1027

Designed for use at clock frequencies to 100 MHz minimum (120 MHz typical). Logic performing inputs ($\bar{J}$ and $\bar{K}$) are available, as well as dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 2
DC Output Loading Factor = 25
Power Dissipation = 250 mW typical

* Any $\bar{J}$ or $\bar{K}$ input, not used for $\bar{C}_D$.
** $\bar{C}_D$ obtained by connecting one $\bar{J}$ and one $\bar{K}$ input together.

The $\bar{J}$ and $\bar{K}$ inputs refer to logic levels while the $\bar{C}_D$ input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to a logical "1" only while the $\bar{C}_D$ input is in a logic "1" state. ($\bar{C}_D$ maximum "1" level = V_{CC} −0.6 V). Clock $\bar{C}_D$ is obtained by tying one $\bar{J}$ and one $\bar{K}$ input together.

R-S TRUTH TABLE

	R	S	Q^{n+1}
Pin No.	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\bar{J}$-$\bar{K}$ Inputs Are Static

$\bar{J}_D$-$\bar{K}_D$ TRUTH TABLE

	$\bar{J}_D$	$\bar{K}_D$	Q^{n+1}
Pin No.	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\bar{Q}^n$

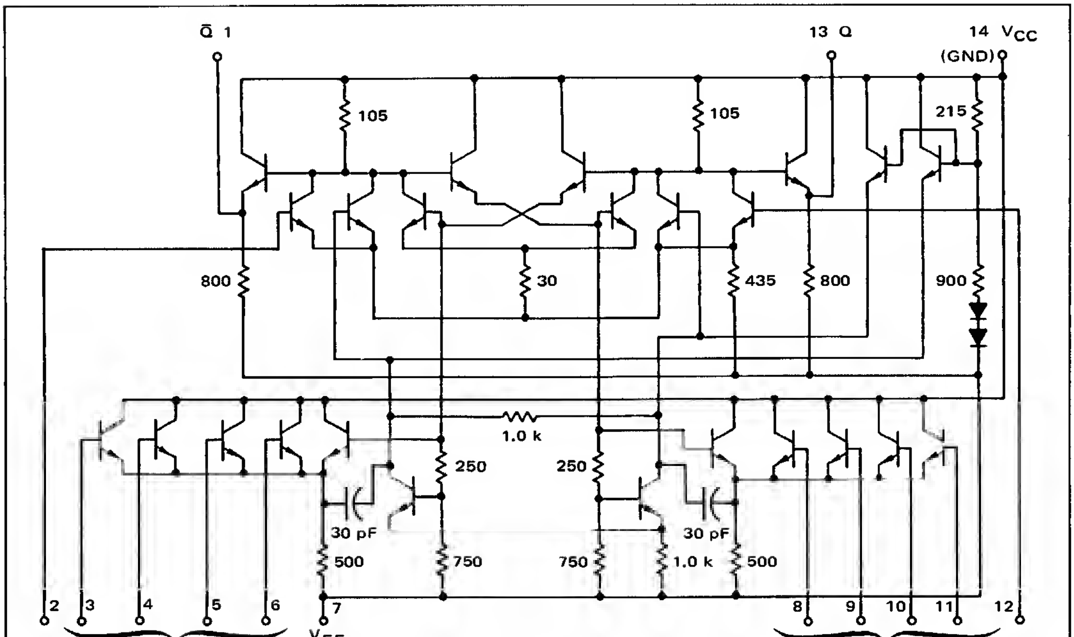
All Other $\bar{J}$-$\bar{K}$ Inputs And The R-S Inputs Are At a "0" Level

CLOCKED $\bar{J}$-$\bar{K}$ TRUTH TABLE

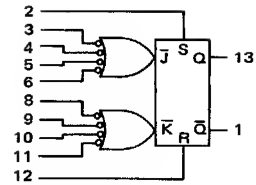
	$\bar{J}$	$\bar{K}$	$\bar{C}_D$	Q^n
Pin No.	*	*	**	13
	ϕ	ϕ	0	Q^n
	0	0	1	$\bar{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All Other $\bar{J}$-$\bar{K}$ Inputs And The R-S Inputs Are At a "0" Level

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1027 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	58	-	-	mAdc
Input Current	I_{in}	2	-	-	-	200	-	-	μAdc
		3	-	-	-		-	-	
		4	-	-	-		-	-	
		5	-	-	-		-	-	
		6	-	-	-		-	-	
		8	-	-	-		-	-	
		9	-	-	-		-	-	
		10	-	-	-		-	-	
		11	-	-	-		-	-	
		12	-	-	-		-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	1.0	-	5.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	13	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	13	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q" or "$\bar{Q}$" Latch Voltage	V_L	2	-1.13	-1.31	-1.11	-1.27	-1.04	-1.21	Vdc
		12	-1.13	-1.31	-1.11	-1.27	-1.04	-1.21	Vdc
Input Toggle Frequency (See Figures 3 & 4)	f_{Tog}	13	-	-	100	-	-	-	MHz
Sensitivity (No Toggle)	-	1			See Figure 1				
		13			See Figure 1				
Sensitivity (Toggle)	-	1, 13			See Figure 2				
Switching Times ④			Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{6+1+}	1	4.0	6.0	4.0	6.0	5.0	8.0	ns
	t_{6+1-}	1							
	t_{8+13+}	13							
	t_{8+13-}	13							
Rise Time	t_{1+}	1							
	t_{13+}	13							
Fall Time	t_{1-}	1							
	t_{13-}	13							

* Individually test each input using the pin connections shown.
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA)

① $V_{in(set)} = V_{OH}$ then $V_{OL(max)}$.

② $V_{in(reset)} = V_{OH}$ then $V_{OL(max)}$.

③ Input voltage is adjusted to obtain $dV_{"1"}/dV_{in} = \infty$.

④ AC fan-out = 3

@Test Temperature	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L
	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0%				mAdc
0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Characteristic	Symbol	Pin Under Test	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	dV_{in}	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
Input Current	I_{in}	2	-	-	2	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
		3	-	-	3	2, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	↓
		4	-	-	4	2, 3, 5, 6, 7, 8, 9, 10, 11, 12	-	-	
		5	-	-	5	2, 3, 4, 6, 7, 8, 9, 10, 11, 12	-	-	
		6	-	-	6	2, 3, 4, 5, 7, 8, 9, 10, 11, 12	-	-	
		8	-	-	8	2, 3, 4, 5, 6, 7, 9, 10, 11, 12	-	-	
		9	-	-	9	2, 3, 4, 5, 6, 7, 8, 10, 11, 12	-	-	
		10	-	-	10	2, 3, 4, 5, 6, 7, 8, 9, 11, 12	-	-	
		11	-	-	11	2, 3, 4, 5, 6, 7, 8, 9, 10, 12	-	-	
		12	-	-	12	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	13	-	-	2 ①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	13	-	14
"Q" Logical "0" Output Voltage	V_{OL}	13	-	-	12 ②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	-	-	14
"$\overline{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-	-	12 ②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1	-	14
"$\overline{Q}$" Logical "0" Output Voltage	V_{OL}	1	-	-	2 ①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
"Q" or "$\overline{Q}$" Latch Voltage	V_L	2	-	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11	-	2 ③	14
		12	-	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11	-	12 ③	14
			Pulse In	Pulse Out					
Input Toggle Frequency (See Figures 3 & 4)	f_{Tog}	13	6, 8	13	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	-	14
Sensitivity (No Toggle)	-	1	6, 8	1	-	↓	-	-	14
		13	6, 8	13	-		-	-	↓
Sensitivity (Toggle)	-	1, 13	6, 8	1, 13	-		-	-	
Switching Times ④						V_{EE} = −4.0 Vdc			+1.2V
Propagation Delay	t_{6+1+}	1	6	1	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	-	14
	t_{6+1-}	1	6	1	-	↓	-	-	↓
	t_{8+13+}	13	8	13	-		-	-	
	t_{8+13-}	13	8	13	-		-	-	
Rise Time	t_{1+}	1	6	1	-		-	-	
	t_{13+}	13	8	13	-		-	-	
Fall Time	t_{1-}	1	6	1	-		-	-	
	t_{13-}	13	8	13	-		-	-	

FIGURE 1 - SENSITIVITY (NO TOGGLE)

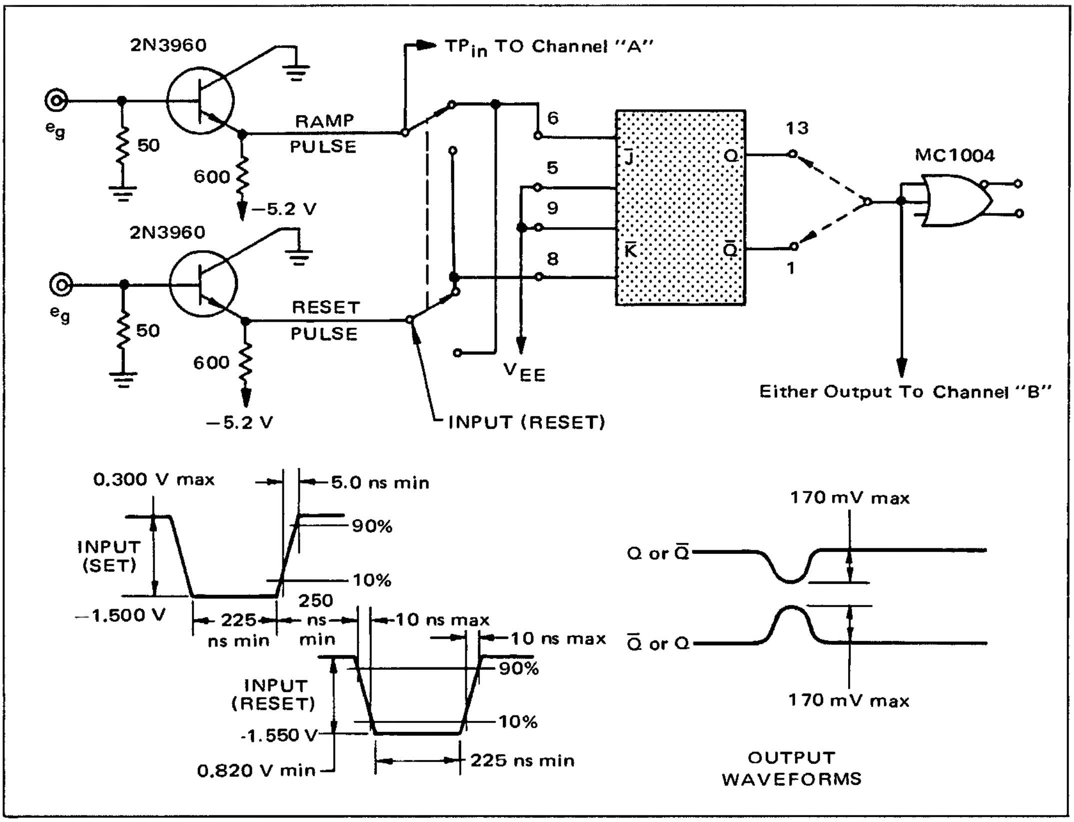
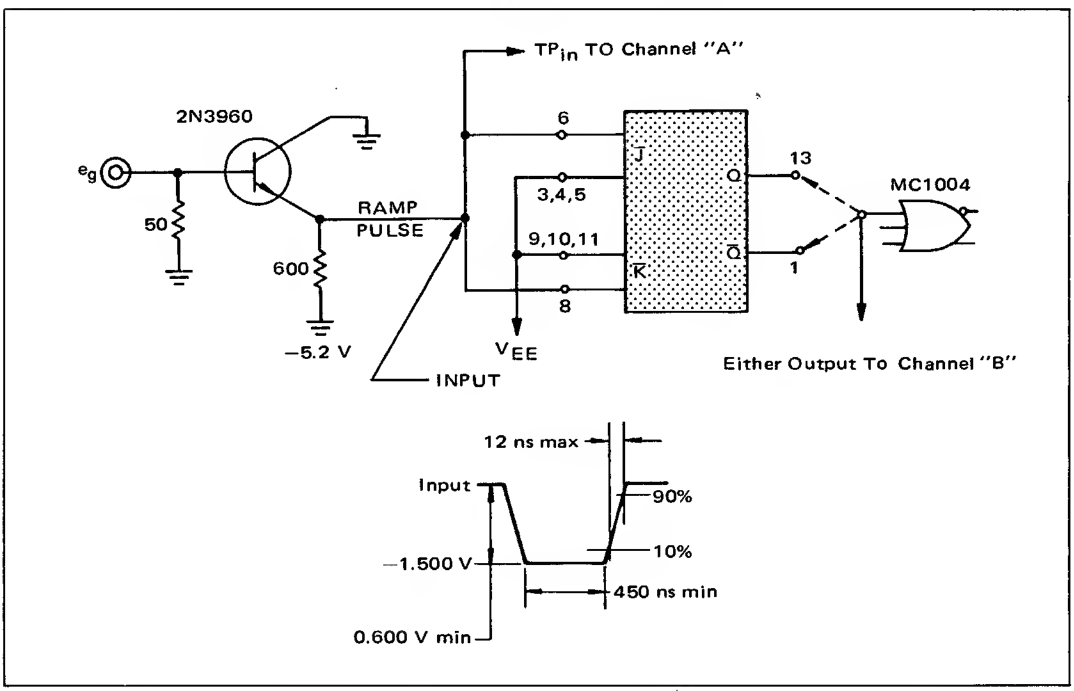


FIGURE 2 - SENSITIVITY (TOGGLE)



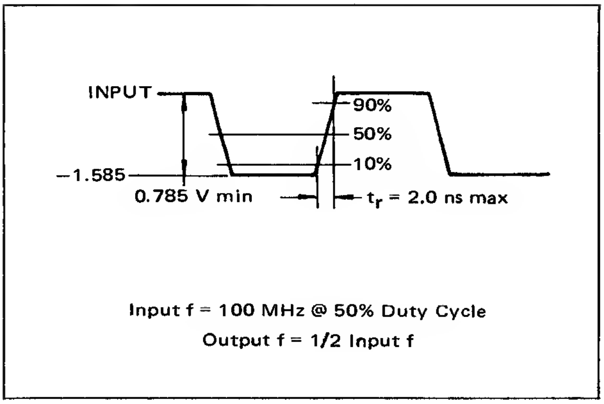
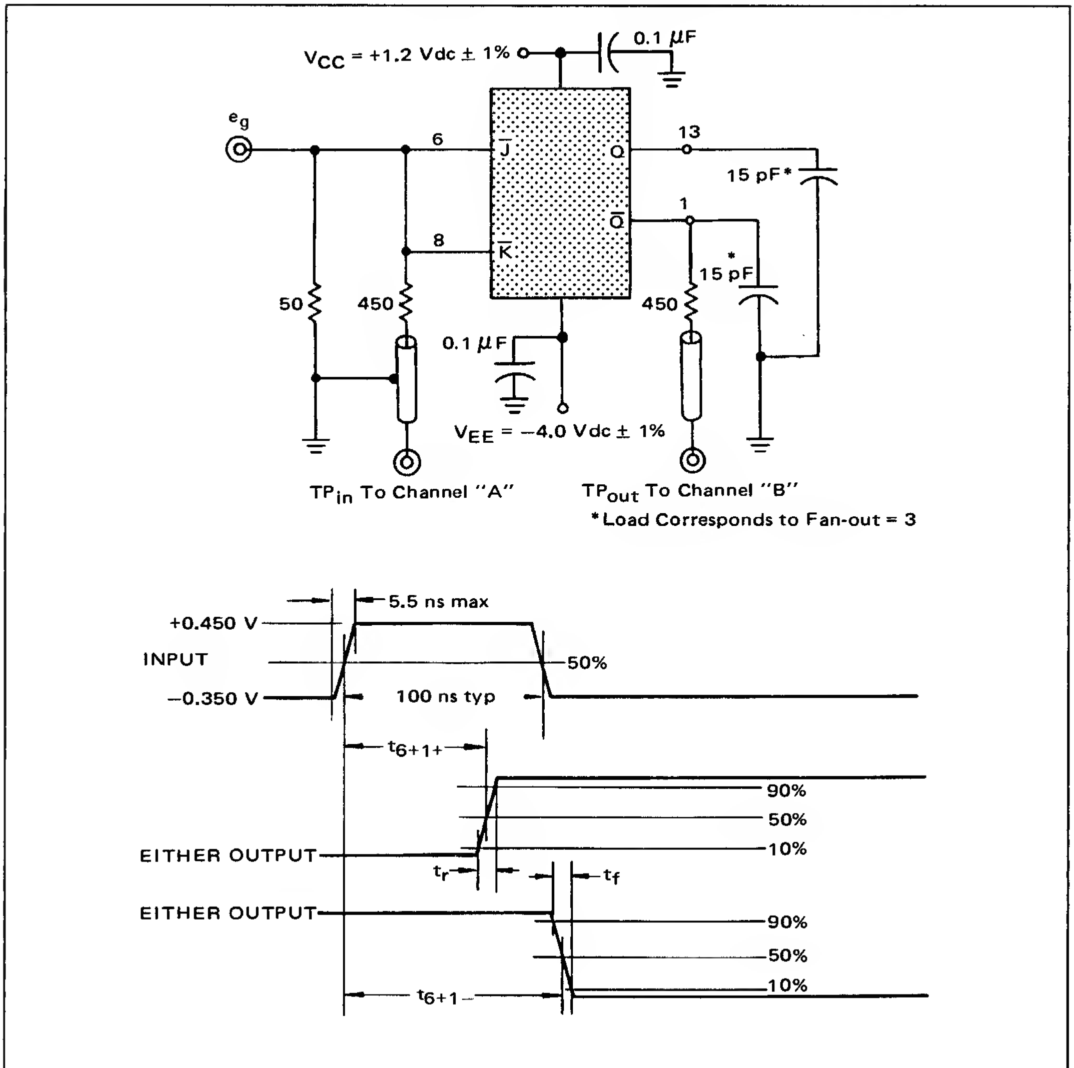


FIGURE 3 - INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

FIGURE 4 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



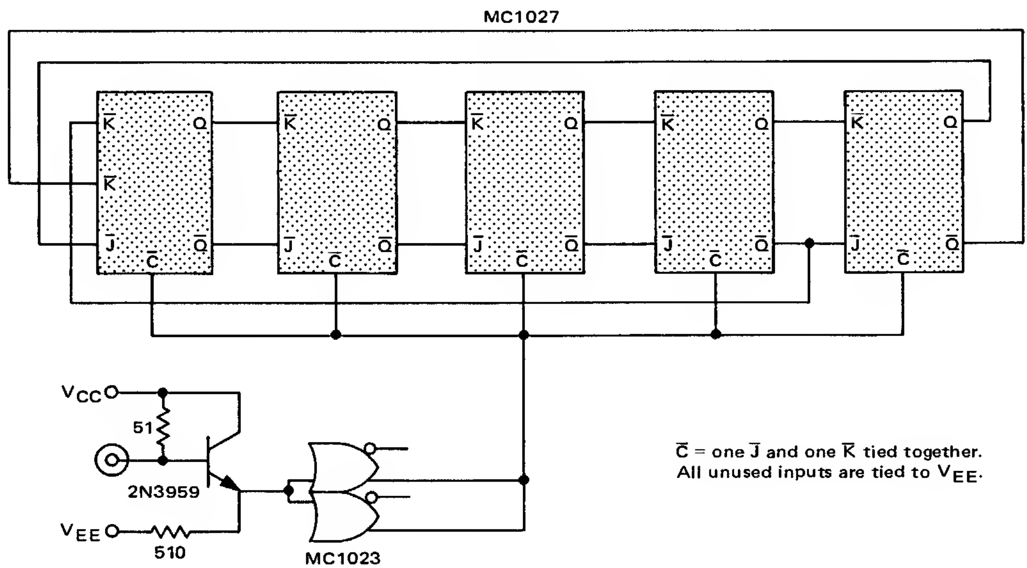
APPLICATIONS INFORMATION

The MC1027 flip-flop is obtained by reducing all resistor values of the MC1013 by a factor of two. The resultant flip-flop is no longer limited by circuit design, but by device speeds. Typically the MC1027 will operate 50% faster than the MC1013. Power dissipation is doubled over that of the MC1013, but circuit operation is the same. The MC1023 clock driver is recommended for driving the MC1027 to its full capability. (The MC1023 high-speed clock driver exhibits propagation delay and rise times of about 2.0 ns when driving five flip-flops.) Maximum operating frequency depends upon layout techniques. Short lead lengths with low impedance lines are recommended. A 100+MHz shift counter is shown in Figure 5.

Operation of the MC1027 is very uniform with negligible variation observed with temperature change from 0°C to +75°C. Propagation delay is nominally 4.5 ns, with rise and fall times varying from 3.5 to 4.0 ns with a load of another flip-flop on the output.

FIGURE 5 - 100 + MHz "SWITCH-TAIL" RING COUNTER

Shift pattern of five "0"s and five "1"s is assured by logic feedback from the fourth to first stage.



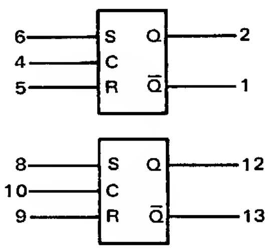
$\bar{C}$ = one $\bar{J}$ and one $\bar{K}$ tied together.
All unused inputs are tied to V_{EE}.

DUAL R-S FLIP-FLOPS
WITH POSITIVE CLOCK

MC1014
MC1214

Two dc Set-Reset flip-flops with a positive clock input provided for each flip-flop. This device is useful as a dual storage element and may be teamed with the MC1015/MC1215 for shift register functions with a minimum number of packages.

POSITIVE LOGIC



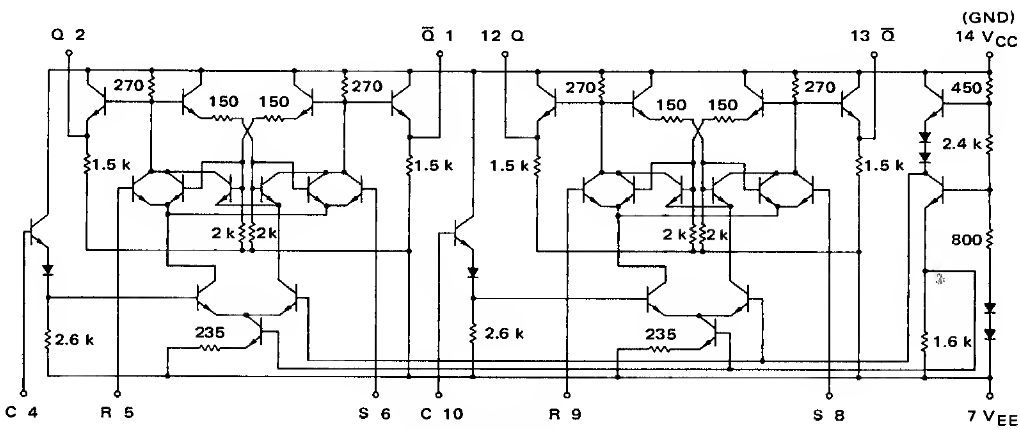
TRUTH TABLE

R	S	C	Q^{n+1}
0	1	1	1
1	0	1	0
0	0	1	Q^n
1	1	1	N.D.
*	*	0	Q^n

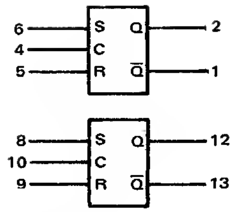
*Either State
N.D. = Not Defined

DC Input Loading Factor: C = 1; S, R = 1.5
DC Output Loading Factor = 25
Power Dissipation = 140 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1214 Test Limits							MC1014 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	36	-	-	mAdc
Input Current	I_{in}	4 5 6	- - -	- - -	- - -	100 150 150	- - -	- - -	μAdc	- - -	- - -	- - -	100 150 150	- - -	- - -	μAdc
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q̄" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q̄" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Inputs Propagation Delay	t_{4+1-}	1	6.0	9.0	6.0	9.0	7.0	10.5	ns	6.0	9.0	6.0	9.0	6.0	9.5	ns
	t_{4+1+}	1	5.0	8.5	5.0	8.5				5.0	8.5	5.0	8.5			
	t_{4+2+}	2	5.0	8.5	5.0	8.5				5.0	8.5	5.0	8.5			
	t_{4+2-}	2	6.0	9.0	6.0	9.0				6.0	9.0	6.0	9.0			
Rise Time	t_{1+}	1						10.0						7.0	10.0	
	t_{2+}	2						10.0								
Fall Time	t_{1-}	1	5.0	8.5			8.0	11.5								
	t_{2-}	2	5.0	8.5			8.0	11.5								
Set-Reset Inputs Propagation Delay	t_{6+1-}	1	5.0	8.0	5.0	8.0	7.0	10.5	ns	5.0	8.0	5.0	8.0	6.0	9.0	ns
	t_{5+1+}	1						10.0							8.5	
	t_{6+2+}	2						10.0							8.5	
	t_{5+2-}	2						10.5							9.0	
Rise Time	t_{1+}	1	6.0	9.0	6.0	9.0	8.0	10.0		6.0	9.0	6.0	9.0	7.0	9.5	
	t_{2+}	2	6.0	9.0	6.0	9.0	8.0	10.0		6.0	9.0	6.0	9.0	7.0	9.5	
Fall Time	t_{1-}	1	5.0	8.5	5.0	8.5	7.0	11.5		5.0	8.5	5.0	8.5	6.0	10.0	
	t_{2-}	2	5.0	8.5	5.0	8.5	7.0	11.5		5.0	8.5	5.0	8.5	6.0	10.0	

* Individually test each input using the pin connections shown.
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

APPLICATIONS INFORMATION

The MC1014/MC1214 is a dual R-S flip-flop with a positive clock input for each flip-flop. An extra level of gating is accomplished with only 2.0 ns increase in propagation delay. This device may be used with the MC1015/MC1215 negative-clock R-S flip-flop in a single-phase clocked master-slave type of shift register as shown in Figure 1.

	@Test Temperature	TEST VOLTAGE/CURRENT VALUES					
		Vdc ±1.0%				V ± 50 mV	mAdc
		$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	V_{BB}	I_L
MC1214	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-1.270	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-1.025	-2.5
MC1014	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-1.210	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-1.115	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	V_{BB}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	4, 10	-	5, 6, 7, 8, 9	-	-	14
Input Current	I_{in}	4	-	-	4	5, 6, 7, 8, 9, 10	-	-	14
		5	-	-	4, 5	6, 7, 8, 9, 10	-	-	14
		6	-	-	4, 6	5, 7, 8, 9, 10	-	-	14
Input Leakage Current	I_R	Inputs*	-	-	-	4, 5, 6, 7, 8, 9, 10	-	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	2	-	4, 6	-	5, 7, 8, 9, 10	5	2	14
"Q" Logical "0" Output Voltage	V_{OL}	2	-	4, 5	-	4, 7, 8, 9, 10	6	-	14
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-	4, 5	-	4, 7, 8, 9, 10	6	1	14
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	-	4, 6	-	5, 7, 8, 9, 10	5	-	14
Switching Times (Fan-Out = 3)			Pulse In	$V_{IH\,min}$ +1.2 Vdc	Pulse Out	V_{EE} = −4.0 Vdc			(+1.2V)
Clock Inputs Propagation Delay	t_{4+1-}	1	4	-	1	5, 6, 7, 8, 9, 10	-	-	14
	t_{4+1+}	1		-	1		-	-	
	t_{4+2+}	2		-	2		-	-	
	t_{4+2-}	2		-	2		-	-	
Rise Time	t_{1+}	1		-	1		-	-	
	t_{2+}	2		-	2		-	-	
Fall Time	t_{1-}	1		-	1		-	-	
	t_{2-}	2		-	2		-	-	
Set-Reset Inputs Propagation Delay	t_{6+1-}	1	6	4	-	7, 8, 9, 10	-	-	14
	t_{5+1+}	1	5		1		-	-	
	t_{6+2+}	2	6		2		-	-	
	t_{5+2-}	2	5		2		-	-	
Rise Time	t_{1+}	1	6		1		-	-	
	t_{2+}	2			2		-	-	
Fall Time	t_{1-}	1			1		-	-	
	t_{2-}	2			2		-	-	

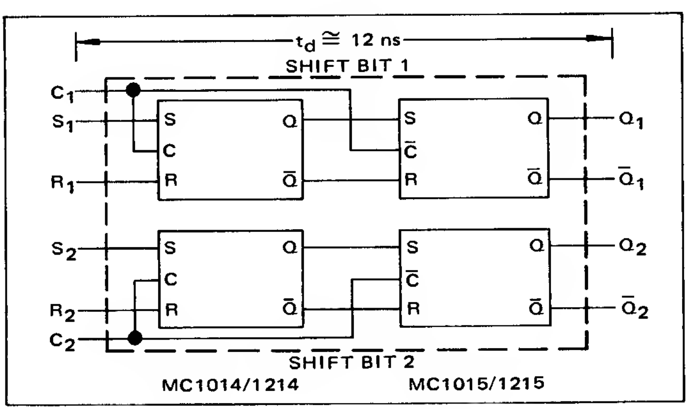
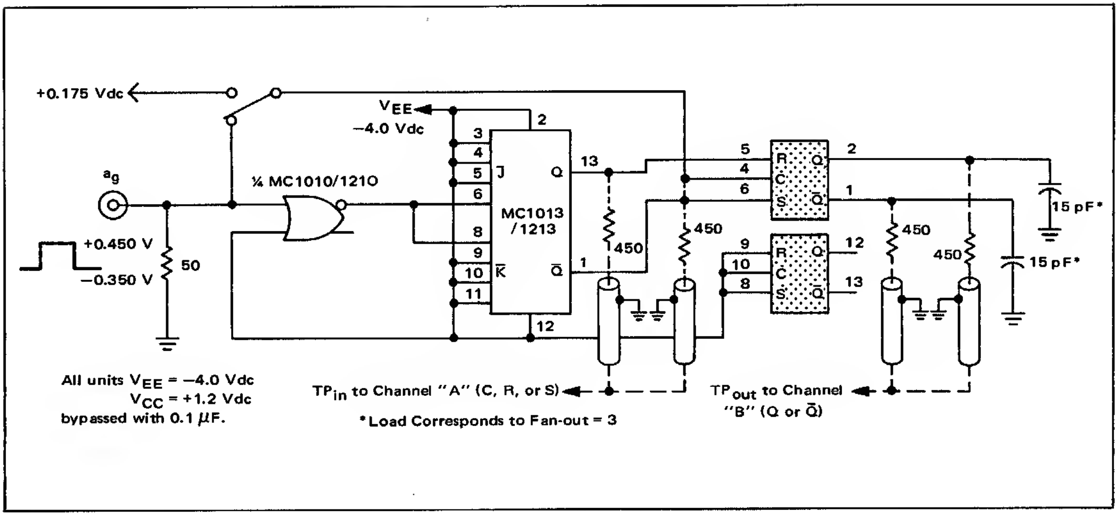
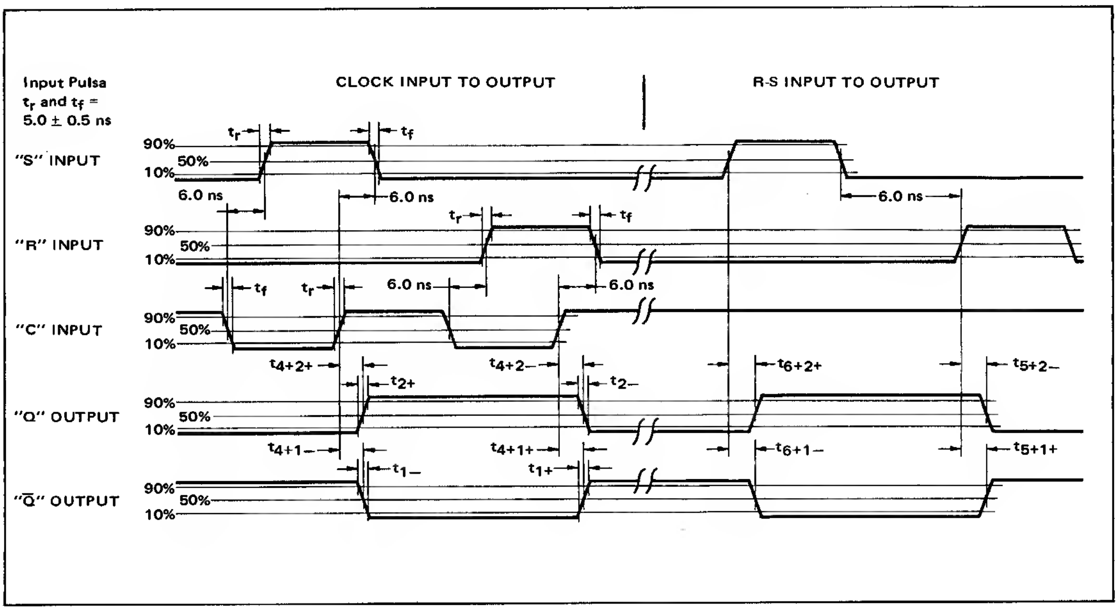


FIGURE 1 - MC1014/MC1214 AND MC1015/MC1215 CONNECTED TO MAKE TWO MASTER-SLAVE SHIFT REGISTER ELEMENTS

SWITCHING TIME TEST CIRCUIT
$T_A = 25^oC$



SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM

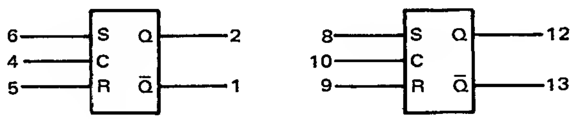


DUAL R-S FLIP-FLOPS
WITH NEGATIVE CLOCK

MC1015
MC1215

Two dc Set-Reset flip-flops with a negative clock input provided for each flip-flop. This unit is useful as a dual storage element and may be teamed with the MC1014/MC1214 for shift register functions with a minimum number of packages.

POSITIVE LOGIC



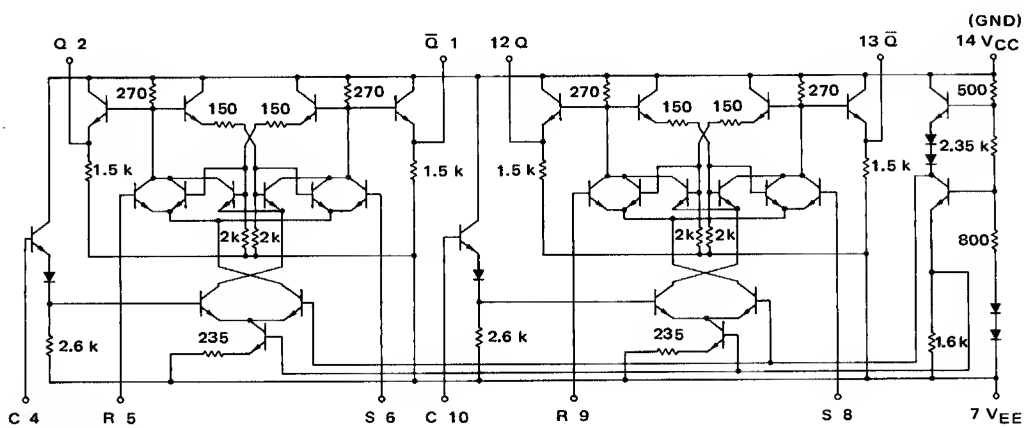
DC Input Loading Factor : C = 1; S, R = 1.5
DC Output Loading Factor = 25
Power Dissipation = 140 mW typical

TRUTH TABLE

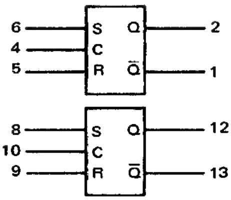
R	S	C	Q^{n+1}
0	1	0	1
1	0	0	0
0	0	0	Q^n
1	1	0	N.D.
*	*	1	Q^n

*Either State
N.D. = Not Defined

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1215 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1015 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	36	-	-	mAdc
Input Current	I_{in}	4	-	-	-	100	-	-	µAdc	-	-	-	100	-	-	µAdc
		5	-	-	-	150	-	-	↓	-	-	-	150	-	-	↓
		6	-	-	-	150	-	-	↓	-	-	-	150	-	-	↓
Input Leakage Current	Inputs*	4,5,6	-	-	-	0.2	-	1.0	µAdc	-	-	-	0.2	-	1.0	µAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Inputs Propagation Delay	t_{4-1-}	1	6.0	10.0	6.0	10.0	8.0	12.0	ns	6.0	10.0	6.0	10.0	7.0	11.0	ns
	t_{4-1+}	1	5.0	8.5	5.0	8.5	7.0	10.5	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
	t_{4-2+}	2	5.0	8.5	5.0	8.5	7.0	10.5	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
	t_{4-2-}	2	6.0	10.0	6.0	10.0	8.0	12.0	↓	6.0	10.0	6.0	10.0	7.0	11.0	↓
Rise Time	t_{1+}	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	t_{2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
Fall Time	t_{1-}	1	5.0	8.5	5.0	8.5	7.0	11.0	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
	t_{2-}	2	5.0	8.5	5.0	8.5	7.0	11.0	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
Set-Reset Inputs Propagation Delay	t_{6+1-}	1	5.0	8.0	5.0	8.0	7.0	11.0	ns	5.0	8.0	5.0	8.0	6.0	9.0	ns
	t_{5+1+}	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	t_{6+2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	t_{5+2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
Rise Time	t_{1+}	1	6.0	9.0	6.0	9.0	↓	↓	↓	6.0	9.0	6.0	9.0	7.0	10.0	↓
	t_{2+}	2	6.0	9.0	↓	9.0	↓	↓	↓	↓	9.0	↓	9.0	↓	↓	↓
Fall Time	t_{1-}	1	5.0	8.0	↓	8.5	8.0	11.5	↓	↓	8.5	↓	8.5	↓	↓	↓
	t_{2-}	2	5.0	8.0	↓	8.5	8.0	11.5	↓	↓	8.5	↓	8.5	↓	↓	↓

* Individually test each input using the pin connections shown.
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

APPLICATIONS INFORMATION

The MC1015/MC1215 is a dual R-S flip-flop with a negative clock input for each flip-flop. An extra level of gating is accomplished with only 2.0 ns increase in propagation delay. This device may be used with the MC1014/MC1214 positive-clock R-S flip-flop in a single-phase clocked master-slave type of shift register as shown in Figure 1.

	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	±50 mV V_{BB}	mAdc I_L
MC1215	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-1.270	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-1.025	-2.5
MC1015	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-1.210	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-1.115	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	V_{BB}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	4, 10	-	5, 6, 7, 8, 9	-	-	14
Input Current	I_{in}	4	-	-	4	5, 6, 7, 8, 9, 10	-	-	14
		5	-	-	5	4, 6, 7, 8, 9, 10	-	-	14
		6	-	-	6	4, 5, 7, 8, 9, 10	-	-	14
Input Leakage Current	Inputs*	4, 5, 6	-	-	-	4, 5, 6, 7, 8, 9, 10	-	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	2	4	6	-	5, 7, 8, 9, 10	5	2	14
"Q" Logical "0" Output Voltage	V_{OL}	2	4	5	-	4, 7, 8, 9, 10	6	-	14
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	4	5	-	4, 7, 8, 9, 10	6	1	14
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	4	6	-	5, 7, 8, 9, 10	5	-	14
			$V_{IL\,max}$ +1.2 Vdc	Pulse In	Pulse Out	V_{EE} = −4.0 Vdc			+1.2V
Switching Times (Fan-Out = 3) Clock Inputs Propagation Delay	t_{4-1-}	1	-	4	1	5, 6, 7, 8, 9, 10	-	-	14
	t_{4-1+}	1	-		1		-	-	
	t_{4-2+}	2	-		2		-	-	
	t_{4-2-}	2	-		2		-	-	
Rise Time	t_{1+}	1	-		1		-	-	
	t_{2+}	2	-		2		-	-	
Fall Time	t_{1-}	1	-		1		-	-	
	t_{2-}	2	-		2		-	-	
Set-Reset Inputs Propagation Delay	t_{6+1-}	1	4	6	1	7, 8, 9, 10	-	-	14
	t_{5+1+}	1		5	1		-	-	
	t_{6+2+}	2		6	2		-	-	
	t_{5+2-}	2		5	2		-	-	
Rise Time	t_{1+}	1		6	1		-	-	
	t_{2+}	2			2		-	-	
Fall Time	t_{1-}	1			1		-	-	
	t_{2-}	2			2		-	-	

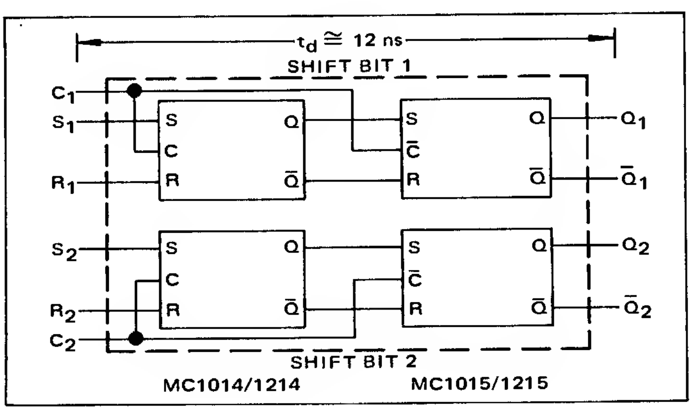
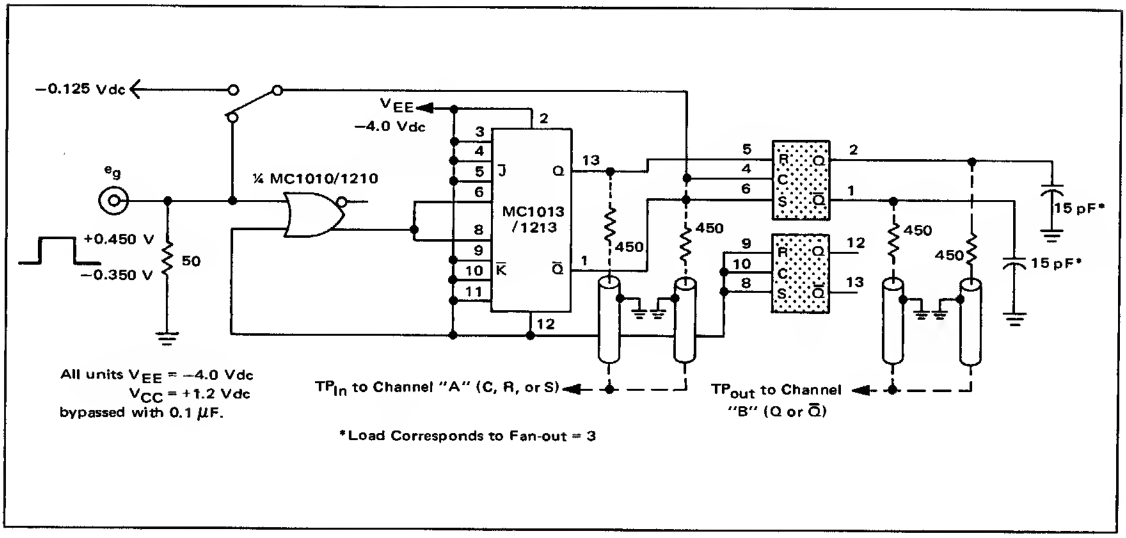
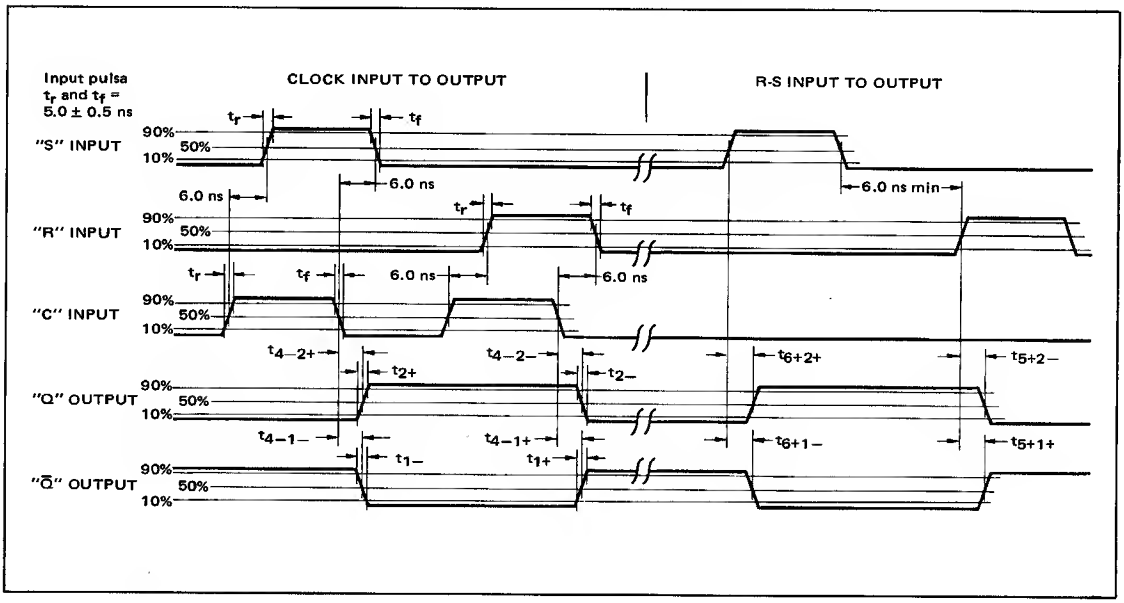


FIGURE 1 - MC1014/MC1214 AND MC1015/MC1215 CONNECTED TO MAKE TWO MASTER-SLAVE SHIFT REGISTER ELEMENTS

SWITCHING TIME TEST CIRCUIT
$T_A = 25^oC$



SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM

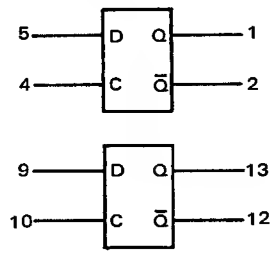


DUAL R-S FLIP-FLOPS
WITH SINGLE RAIL INPUT
AND NEGATIVE CLOCK

MC1016
MC1216

Two dc storage flip-flops with a positive clock input provided for each flip-flop. This device is useful as a dual storage element requiring only a single rail input, as a memory data register, a sample and hold register, or as a clocked R-S flip-flop with no undefined logic state.

POSITIVE LOGIC

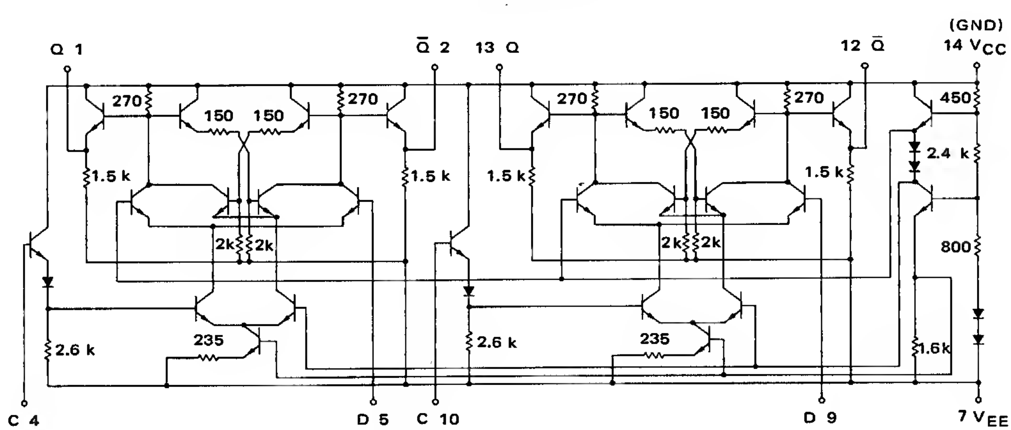


DC Input Loading Factor : C = 1; D = 1.5
DC Output Loading Factor = 25
Power Dissipation = 140 mW typical

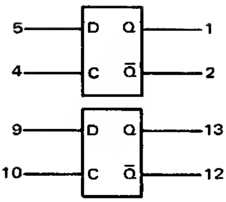
TRUTH TABLE

D	C	Q^{n+1}
0	0	Q^n
1	0	Q^n
0	1	0
1	1	1

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1216 Test Limits −55°C Min	Max	+25°C Min	Max	+125°C Min	Max	Unit	MC1016 Test Limits 0°C Min	Max	+25°C Min	Max	+75°C Min	Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	36	-	-	mAdc
Input Current	I_{in}	4	-	-	-	100	-	-	µAdc	-	-	-	100	-	-	µAdc
		5	-	-	-	150	-	-	µAdc	-	-	-	150	-	-	µAdc
Input Leakage Current	I_R	4	-	-	-	0.2	-	1.0	µAdc	-	-	-	0.2	-	1.0	µAdc
		5	-	-	-	0.2	-	1.0	µAdc	-	-	-	0.2	-	1.0	µAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q̄" Logical "1" Output Voltage‡	V_{OH}‡	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q̄" Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Inputs Propagation Delay	t_{4+1-}	1	6.0	9.0	6.0	9.0	7.0	10.5	ns	6.0	9.0	6.0	9.0	6.0	9.5	ns
	t_{4+1+}	1	5.0	8.0	5.0	8.0	6.0	9.5	↓	5.0	8.0	5.0	8.0	5.0	8.5	↓
	t_{4+2+}	2	5.0	8.0	5.0	8.0	6.0	9.5	↓	5.0	8.0	5.0	8.0	5.0	8.5	↓
	t_{4+2-}	2	6.0	9.0	6.0	9.0	7.0	10.5	↓	6.0	9.0	6.0	9.0	6.0	9.5	↓
Rise Time	t_{1+}	1	5.0	7.5	5.0	7.5	6.0	9.5	↓	5.0	7.5	5.0	7.5	5.0	8.0	↓
	t_{2+}	2	5.0	7.5	5.0	7.5	6.0	9.5	↓	5.0	7.5	5.0	7.5	5.0	8.0	↓
Fall Time	t_{1-}	1	6.0	8.5	6.0	8.5	7.0	10.5	↓	6.0	8.5	6.0	8.5	6.0	9.5	↓
	t_{2-}	2	5.0	8.5	5.0	8.5	7.0	10.5	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
Set Inputs Propagation Delay	t_{5+1+}	1	5.0	8.0	5.0	8.0	6.0	9.5	ns	5.0	8.0	5.0	8.0	5.0	8.5	ns
	t_{5-1-}	1	↓	↓	↓	↓	7.0	10.5	↓	↓	↓	↓	↓	↓	↓	↓
	t_{5+2-}	2	↓	↓	↓	↓	7.0	10.5	↓	↓	↓	↓	↓	↓	↓	↓
	t_{5-2+}	2	↓	↓	↓	↓	6.0	9.5	↓	↓	↓	↓	↓	↓	↓	↓
Rise Time	t_{1+}	1	↓	7.5	↓	7.5	↓	9.0	↓	↓	7.5	↓	7.5	↓	8.0	↓
	t_{2+}	2	↓	7.5	↓	7.5	↓	9.0	↓	↓	7.5	↓	7.5	↓	8.0	↓
Fall Time	t_{1-}	1	↓	8.5	6.0	9.0	8.0	11	↓	6.0	9.0	6.0	9.0	7.0	10	↓
	t_{2-}	2	↓	8.5	6.0	9.0	8.0	11	↓	6.0	9.0	6.0	9.0	7.0	10	↓

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

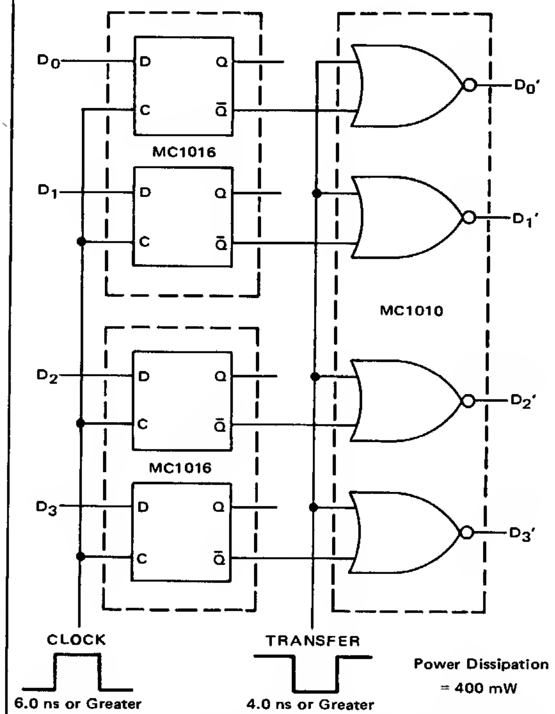
@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	mAdc I_L
MC1216	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1016	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Characteristic	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	-	4, 10	-	5, 7, 9	-	14
Input Current	-	-	4	5, 7, 9, 10	-	14
	-	-	4, 5	7, 9, 10	-	14
Input Leakage Current	-	-	-	4, 5, 7, 9, 10	-	14
	-	-	-	4, 5, 7, 9, 10	-	14
"Q" Logical "1" Output Voltage‡	-	4, 5	-	7, 9, 10	1	14
"Q" Logical "0" Output Voltage	5	4	-	7, 9, 10	-	14
"$\bar{Q}$" Logical "1" Output Voltage‡	5	4	-	7, 9, 10	2	14
"$\bar{Q}$" Logical "0" Output Voltage	-	4, 5	-	7, 9, 10	-	14
Switching Times (Fan-Out = 3)	Pulse In	$V_{IH\,min}$ +1.2 Vdc	Pulse Out	V_{EE} = −4.0 Vdc		(+1.2V)
Clock Inputs Propagation Delay	4	-	1	7, 9, 10	-	14
	↓	-	1	↓	-	↓
	↓	-	2	↓	-	↓
	↓	-	2	↓	-	↓
Rise Time	↓	-	1	↓	-	↓
	↓	-	2	↓	-	↓
Fall Time	↓	-	1	↓	-	↓
	↓	-	2	↓	-	↓
Set Inputs Propagation Delay	5	4	1	7, 9, 10	-	14
	↓	↓	1	↓	-	↓
	↓	↓	2	↓	-	↓
	↓	↓	2	↓	-	↓
Rise Time	↓	↓	1	↓	-	↓
	↓	↓	2	↓	-	↓
Fall Time	↓	↓	1	↓	-	↓
	↓	↓	2	↓	-	↓

APPLICATIONS INFORMATION

The MC1016/MC1216 is a single-rail storage element that has no undefined logic state. (Note the change in the truth table over that of the dual-rail type of device, such as MC1014/MC1214 or MC1015/MC1215.) The speed-power product is better than that obtained with any other bipolar technique. An example of a 4-bit storage register with both input and output gating is shown in Figure 1, and an 8-bit buffer register with input gating is shown in Figure 2.



Power Dissipation = 400 mW

t_{pd} from D_0 to D_0' – Typically 8.0 ns with transfer low and clock high
t_{pd} from C to D_0' – Typically 9.0 ns with transfer low and clock going to high level

FIGURE 1 - 4-BIT STORAGE REGISTER WITH GATED INPUTS AND OUTPUTS (THREE DEVICES)

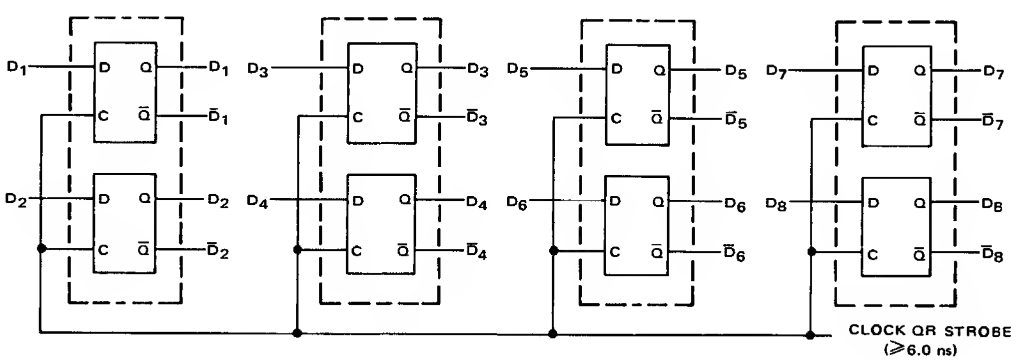
FIGURE 2 - 8-BIT BUFFER REGISTER WITH INPUT GATING (FOUR DEVICES)

TRUTH TABLE

D	C	Q^{n+1}	$\bar{Q}^{n+1}$
ϕ	0	Q^n	$\bar{Q}^n$
0	1	0	1
1	1	1	0

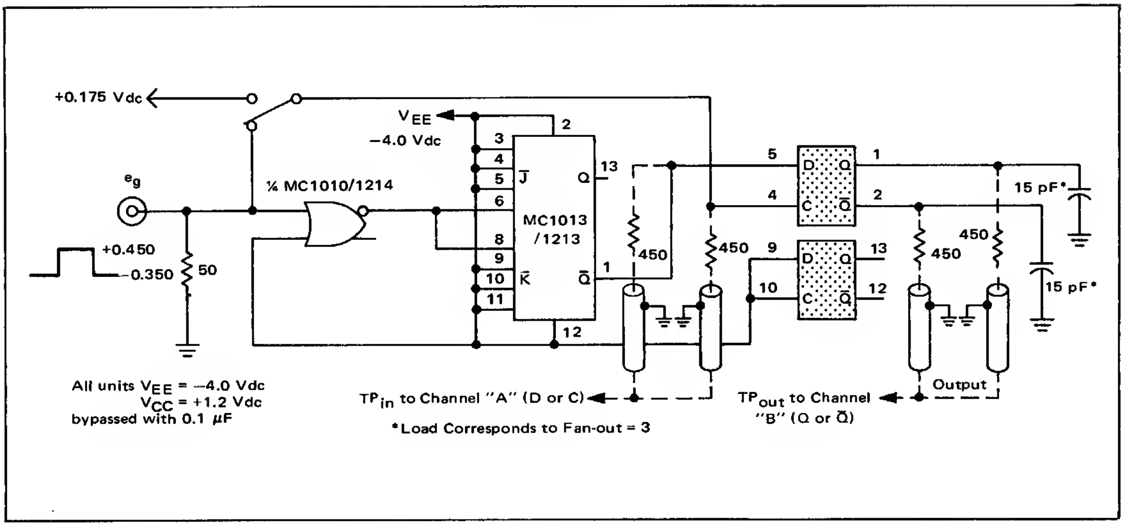
ϕ = Either state may be present

t_{pd} from D_{in} to Q or $\bar{Q} \approx 4.0$ ns
t_{pd} from C_{in} to Q or $\bar{Q} \approx 6.0$ ns

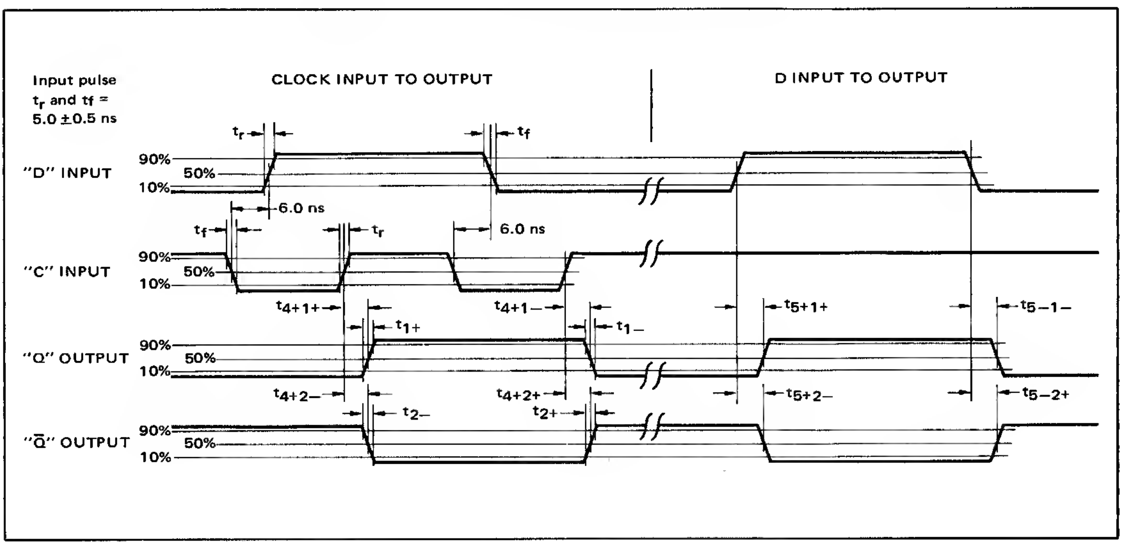


SWITCHING TIME TEST CIRCUIT

$T_A = 25^oC$



SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM



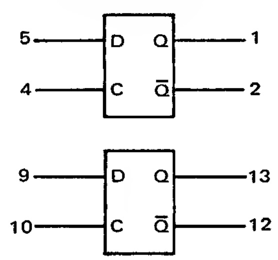
DUAL R-S FLIP-FLOPS WITH SINGLE RAIL INPUT AND POSITIVE CLOCK

MECL II MC1000/1200 series

MC1033
MC1233

Two dc storage flip-flops with a negative clock input provided for each flip-flop. This device is useful as a dual storage element requiring only a single rail input, as a memory data register, a sample and hold register, or as a clocked R-S flip-flop with no undefined logic state. It may be teamed with the MC1016/MC1216 for shift register functions with a minimum number of packages.

POSITIVE LOGIC

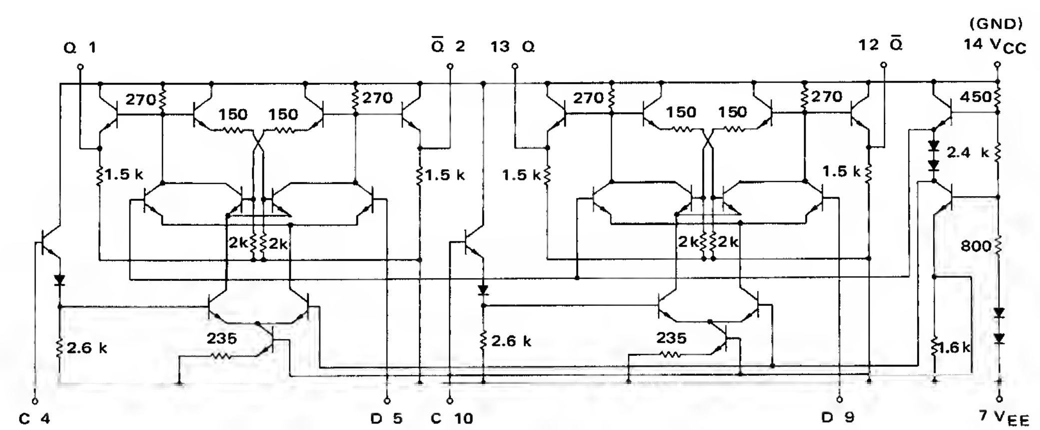


TRUTH TABLE

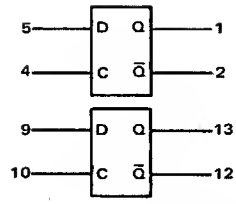
D	C	Q^{n+1}
0	1	Q^n
1	1	Q^n
0	0	0
1	0	1

DC Input Loading Factor: C = 1; D = 1.5
DC Output Loading Factor = 25
Power Dissipation = 140 mW typ

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1233 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1033 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	36	-	-	mAdc
Input Current	I_{in}	4	-	-	-	100	-	-	µAdc	-	-	-	100	-	-	µAdc
		5	-	-	-	150	-	-	µAdc	-	-	-	150	-	-	µAdc
Input Leakage Current	I_R	4	-	-	-	0.2	-	1.0	µAdc	-	-	-	0.2	-	1.0	µAdc
		5	-	-	-	0.2	-	1.0	µAdc	-	-	-	0.2	-	1.0	µAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q̄" Logical "1" Output Voltage‡	V_{OH}‡	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q̄" Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times* (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Inputs Propagation Delay	t_{4-1+}	1	6.0	8.5	6.0	8.5	8.0	10.5	ns	6.0	8.5	6.0	8.5	7.0	9.5	ns
	t_{4-1-}	1	5.0	10	5.0	10	7.0	12		5.0	10	5.0	10	6.0	11	
	t_{4-2+}	2	5.0	8.5	5.0	8.5	7.0	10.5		5.0	8.5	5.0	8.5	6.0	9.5	
	t_{4-2-}	2	6.0	10	6.0	10	8.0	12		6.0	10	6.0	10	7.0	11	
Rise Time	t_{1+}	1														
	t_{2+}	2	↓	↓	↓	↓	↓	↓		↓	↓	↓	↓	↓	↓	
Fall Time	t_{1-}	1	5.0	8.5	5.0	8.5	7.0	11		5.0	8.5	5.0	8.5	6.0	9.5	
	t_{2-}	2	5.0	8.5	5.0	8.5	7.0	11	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
Set Inputs Propagation Delay	t_{5+1+}	1	5.0	8.0	5.0	8.0	6.0	9.5	ns	5.0	8.0	5.0	8.0	5.0	8.5	ns
	t_{5-1-}	1					7.0	10.5								
	t_{5+2-}	2					7.0	10.5								
	t_{5-2+}	2		↓		↓	6.0	9.5			↓		↓		↓	
Rise Time	t_{1+}	1		7.5		7.5		9.0			7.5		7.5		8.0	
	t_{2+}	2		7.5	↓	7.5	↓	9.0		↓	7.5	↓	7.5	↓	8.0	
Fall Time	t_{1-}	1		8.5	6.0	9.0	8.0	11		6.0	9.0	6.0	9.0	7.0	10	
	t_{2-}	2	↓	8.5	6.0	9.0	8.0	11	↓	6.0	9.0	6.0	9.0	7.0	10	↓

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

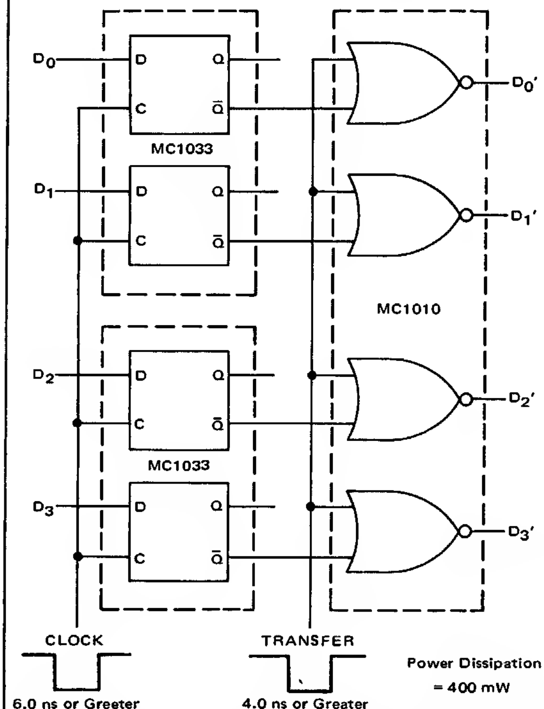
@Test Temperature		TEST VOLTAGE/CURRENT VALUES: Vdc ±1.0% $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	mAdc I_L
MC1233	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1033	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Characteristic	Symbol	Pin Under Test	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	4, 10	-	5, 7, 9	-	14
Input Current	I_{in}	4	-	-	4	5, 7, 9, 10	-	14
		5	-	-	5	4, 7, 9, 10	-	14
Input Leakage Current	I_R	4	-	-	-	4, 5, 7, 9, 10	-	14
		5	-	-	-	4, 5, 7, 9, 10	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	1	4	5	-	7, 9, 10	1	14
"Q" Logical "0" Output Voltage	V_{OL}	1	4, 5	-	-	7, 9, 10	-	14
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	2	4, 5	-	-	7, 9, 10	2	14
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	2	4	5	-	7, 9, 10	-	14
Switching Times* (Fan-Out = 3)			$V_{IL\,max}$ +1.2 Vdc	Pulse In	Pulse Out	V_{EE} = −4.0 Vdc		(+1.2V)
Clock Inputs Propagation Delay	t_{4-1+}	1	4	-	1	7, 9, 10	-	14
	t_{4-1-}	1		-	1		-	
	t_{4-2+}	2		-	2		-	
	t_{4-2-}	2		-	2		-	
Rise Time	t_{1+}	1		-	1		-	
	t_{2+}	2		-	2		-	
Fall Time	t_{1-}	1		-	1		-	
	t_{2-}	2		-	2		-	
Set Inputs Propagation Delay	t_{5+1+}	1	5	4	1	7, 9, 10	-	14
	t_{5-1-}	1			1		-	
	t_{5+2-}	2			2		-	
	t_{5-2+}	2			2		-	
Rise Time	t_{1+}	1			1		-	
	t_{2+}	2			2		-	
Fall Time	t_{1-}	1			1		-	
	t_{2-}	2			2		-	

APPLICATIONS INFORMATION

The MC1033/MC1233 is a single-rail storage element that has no undefined logic state. (Note the change in the truth table over that of the dual-rail type of device, such as MC1014/MC1214 or MC1015/MC1215.) The speed-power product is better than that obtained with any other bipolar technique. An example of a 4-bit storage register with both input and output gating is shown in Figure 1, and an 8-bit buffer register with input gating is shown in Figure 2.



t_{pd} from D_0 to D_0' — Typically 8.0 ns with transfer high and clock low
t_{pd} from C to D_0' — Typically 9.0 ns with transfer high and clock going to low level

FIGURE 1 - 4-BIT STORAGE REGISTER WITH GATED INPUTS AND OUTPUTS (THREE DEVICES)

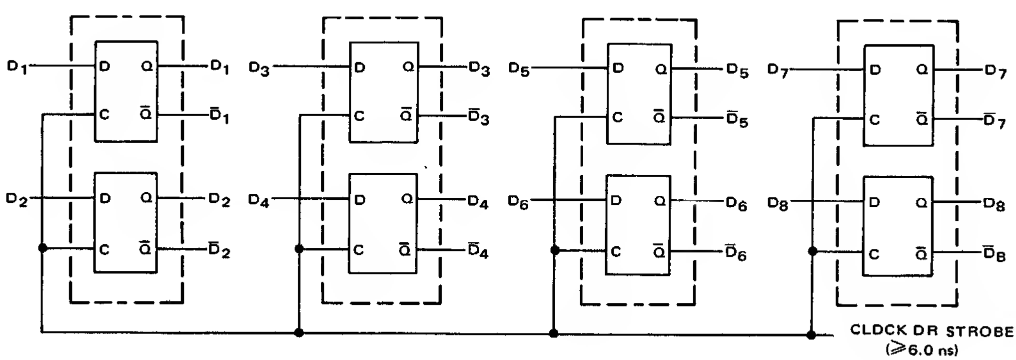
FIGURE 2 - 8-BIT BUFFER REGISTER WITH INPUT GATING (FOUR DEVICES)

TRUTH TABLE

D	C	Q^{n+1}	$\bar{Q}^{n+1}$
ϕ	1	Q^n	$\bar{Q}^n$
0	0	0	1
1	0	1	0

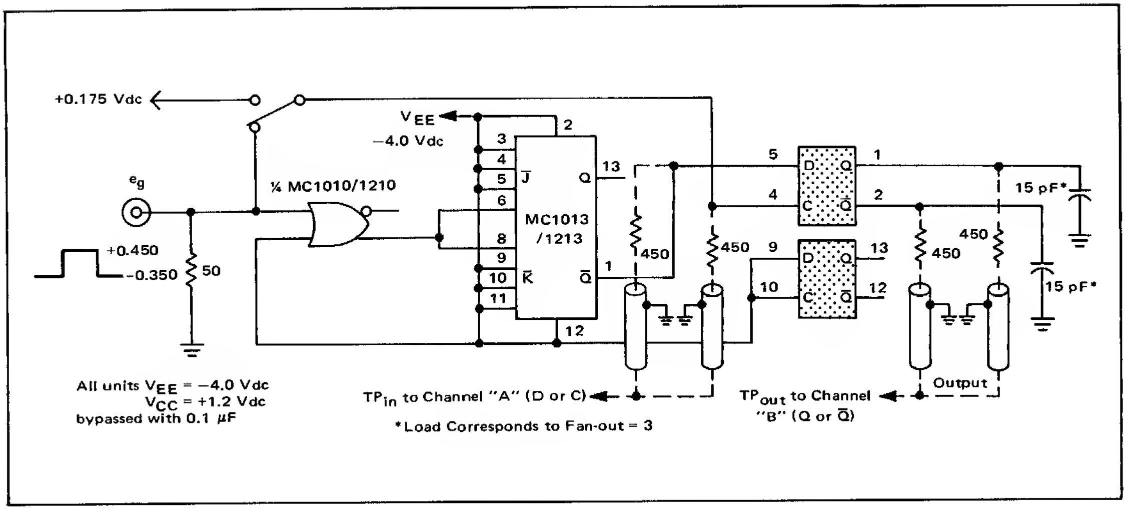
ϕ = Either state may be present

t_{pd} from D_{in} to Q or $\bar{Q} \approx 4.0$ ns
t_{pd} from C_{in} to Q or $\bar{Q} \approx 6.0$ ns

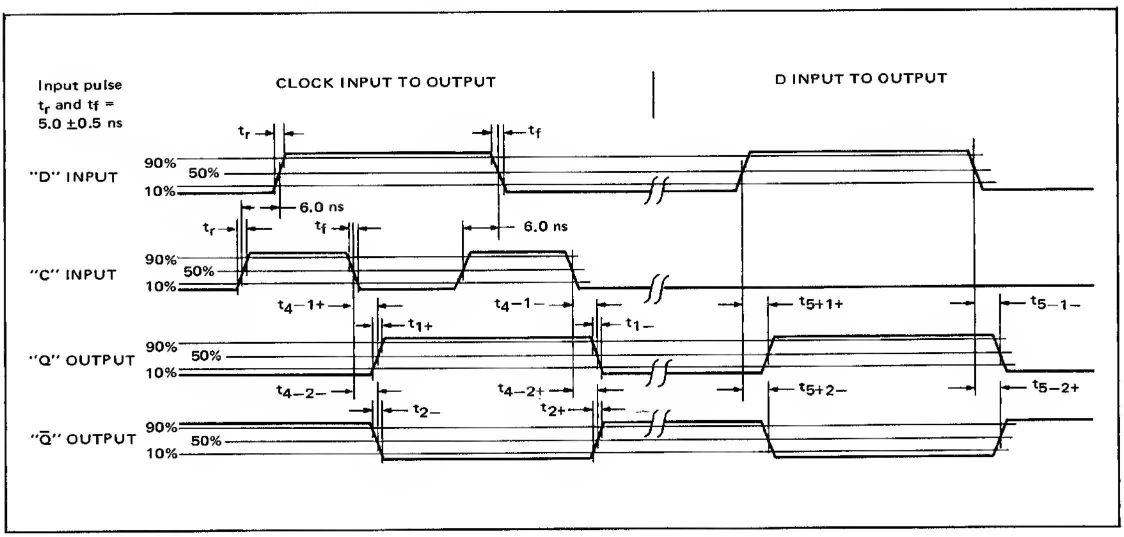


SWITCHING TIME TEST CIRCUIT

$T_A = 25^oC$



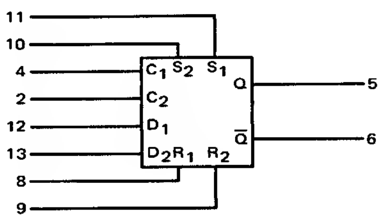
SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM



MC1022
MC1222

Designed for clocked-storage operation based on the "master-slave" principle. Operation depends only on voltage levels, therefore the shape of the clock waveform becomes unimportant in determining the state of the flip-flop. When the clock is low, the input data is stored in the "master" and is subsequently transferred to the "slave" when the clock is high, making the data available at the outputs. In this operation the "master" is disabled before the slave is enabled, due to the design of the internal threshold skew. Along with two data and two Clock inputs, the unit provides two SET and two RESET inputs that are independent of the Clock.

POSITIVE LOGIC



DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 110 mW typical

R-S TRUTH TABLE

	R	S	Q^{n+1}	$\bar{Q}^{n+1}$
Pin No.	8 or 9	10 or 11	5	6
	0	0	Q^n	$\bar{Q}^n$
	0	1	1	0
	1	0	0	1
	1	1	N.D.	N.D.

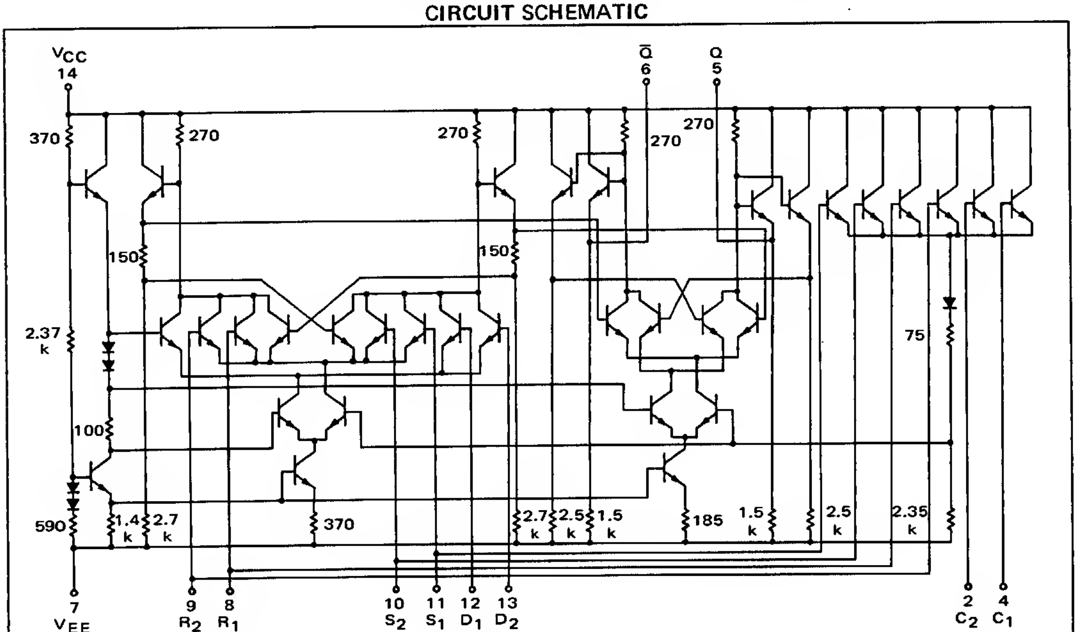
N.D. = Not Defined

CLOCKED TRUTH TABLE

	D	C	Q^{n+1}	$\bar{Q}^{n+1}$
Pin No.	12 or 13	2 or 4	5	6
	0	0	Q^n	$\bar{Q}^n$
	1	0	Q^n	$\bar{Q}^n$
	0	1*	0	1
	1	1*	1	0

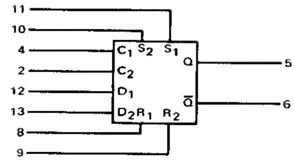
*A "1" or Clock input is defined for this flip-flop as a change in level from a low input to a high input.

CIRCUIT SCHEMATIC



Resistor values are nominal.

ELECTRICAL CHARACTERISTICS



Characteristic	Symbol	Pin Under Test	MC1222 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1022 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	27	-	-	mAdc	-	-	-	27	-	-	mAdc
Input Current	I_{in}	2	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		4	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		8	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		9	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		10	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		11	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		12	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		13	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		5†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		5†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q̄" Logical "1" Output Voltage‡	V_{OH}‡	6	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		6†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q̄" Logical "0" Output Voltage	V_{OL}	6	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		6†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Input Propagation Delay	t_{2+5-}	5	8.0	12	8.0	12	11	15	ns	8.0	12	8.0	12	9.0	13	ns
	t_{2+5+}	5	7.0	11	7.0	11	12	18	↓	7.0	11	7.0	11	9.0	13	↓
	t_{2+6+}	6	7.0	11	7.0	11	12	18	↓	7.0	11	7.0	11	9.0	13	↓
	t_{2+6-}	6	8.0	12	8.0	12	11	15	↓	8.0	12	8.0	12	9.0	13	↓
Rise Time	t_{5+}, t_{6+}	5, 6	5.0	7.5	5.0	8.5	7.0	11	↓	5.0	8.0	5.0	8.5	6.0	9.0	↓
Fall Time	t_{5-}, t_{6-}	5, 6	7.0	9.5	7.0	11.5	8.0	13	↓	7.0	10.5	7.0	11.5	8.0	12	↓
Set Input Propagation Delay	t_{10+5+}	5	8.0	12	8.0	13	10	22	ns	8.0	12	8.0	13	10	14	ns
	t_{10+5+}	5	↓	12	8.0	13	10	22	↓	↓	12	8.0	13	10	14	↓
	t_{10+6-}	6	↓	13	9.0	14	11	19	↓	↓	13	9.0	14	11	15	↓
	t_{10+6-}	6	↓	13	9.0	14	11	19	↓	↓	13	9.0	14	11	15	↓
Reset Input Propagation Delay	t_{9+5-}	5	8.0	13	9.0	14	11	19	ns	8.0	13	9.0	14	11	15	ns
	t_{9+5-}	5	↓	13	9.0	14	11	19	↓	↓	13	9.0	14	11	15	↓
	t_{9+6+}	6	↓	12	8.0	13	10	22	↓	↓	12	8.0	13	10	14	↓
	t_{9+6+}	6	↓	12	8.0	13	10	22	↓	↓	12	8.0	13	10	14	↓

* Individually test each input using the pin connections shown.

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

† Output level to be measured after clock transition on pin 2 or 4 through one positive-going and one negative-going edge. (V_{IH} / V_{IL})

	@Test Temperature	V_{IL}	V_{IH}	$V_{IH\,max}$	V_{EE}	I_L
		TEST VOLTAGE/CURRENT VALUES				
		Vdc ± 1.0%				mAdc
MC1222	−55°C	-1.580	-0.990	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+125°C	-1.380	-0.700	-	-5.2	-2.5
MC1022	0°C	-1.525	-0.895	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+75°C	-1.435	-0.775	-	-5.2	-2.5

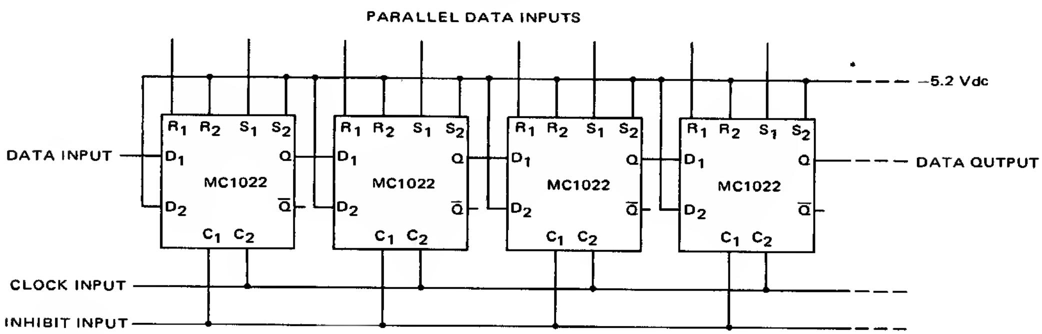
Characteristic	Symbol	Pin Under Test	V_{IL}	V_{IH}	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
			TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					
Power Supply Drain Current	I_E	7	-	-	-	2, 4, 7, 8, 9, 10, 11, 12, 13	-	14
Input Current	I_{in}	2	-	-	2	4, 7, 8, 9, 10, 11, 12, 13	-	14
		4	-	-	4	2, 7, 8, 9, 10, 11, 12, 13	-	↓
		8	-	-	8	2, 4, 7, 9, 10, 11, 12, 13	-	↓
		9	-	-	9	2, 4, 7, 8, 10, 11, 12, 13	-	↓
		10	-	-	10	2, 4, 7, 8, 9, 11, 12, 13	-	↓
		11	-	-	11	2, 4, 7, 8, 9, 10, 12, 13	-	↓
		12	-	-	12	2, 4, 7, 8, 9, 10, 11, 13	-	↓
		13	-	-	13	2, 4, 7, 8, 9, 10, 11, 12	-	↓
Input Leakage Current	I_R	Inputs*	-	-	-	2, 4, 7, 8, 9, 10, 11, 12, 13	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	5	-	10	-	2, 4, 7, 8, 9, 11, 12, 13	5	14
		5†	-	13	-	2, 7, 8, 9, 10, 11, 12	5	14
"Q" Logical "0" Output Voltage	V_{OL}	5	-	9	-	2, 4, 7, 8, 10, 11, 12, 13	-	14
		5†	13	-	-	4, 7, 8, 9, 10, 11, 12	-	14
"$\overline{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	6	-	8	-	2, 4, 7, 9, 10, 11, 12, 13	6	14
		6†	12	-	-	4, 7, 8, 9, 10, 11, 13	6	14
"$\overline{Q}$" Logical "0" Output Voltage	V_{OL}	6	-	11	-	2, 4, 7, 8, 9, 10, 12, 13	-	14
		6†	-	12	-	2, 7, 8, 9, 10, 11, 13	-	14
					Pulse In	V_{EE} — 4.0 Vdc	Pulse Out	(+1.2 Vdc)
Switching Times Clock Input Propagation Delay	t_{2+5-}	5	-	-	2	4,7,8,9,10,11,12,13	5	14
	t_{2+5+}	5	-	-	↓	↓	5	↓
	t_{2+6+}	6	-	-	↓	↓	6	↓
	t_{2+6-}	6	-	-	↓	↓	6	↓
Rise Time	t_{5+}, t_{6+}	5, 6	-	-	↓	↓	5,6	↓
Fall Time	t_{5-}, t_{6-}	5, 6	-	-	↓	↓	5,6	↓
Set Input Propagation Delay	t_{10+5+}	5	-	2	10	4,7,8,11,12,13	5	14
	t_{10+5+}	5	2	-	↓	↓	5	↓
	t_{10+6-}	6	-	2	↓	↓	6	↓
	t_{10+6-}	6	2	-	↓	↓	6	↓
Reset Input Propagation Delay	t_{9+5-}	5	-	2	9	4,7,8,11,12,13	5	14
	t_{9+5-}	5	2	-	↓	↓	5	↓
	t_{9+6+}	6	-	2	↓	↓	6	↓
	t_{9+6+}	6	2	-	↓	↓	6	↓

APPLICATIONS INFORMATION

The MC1022/MC1222 single-phase Type D flip-flop offers advantages over the J-K flip-flop in applications such as single-rail operation. Since a true master-slave design is utilized, the input data may be asynchronous. There is no chance of data "rippling through" if the clock is in the low state. The SET and RESET inputs are also completely independent of the clock and will override the clock, setting both the master and the slave portions of the flip-flop. All the logic inputs are duplicated and ORed together internally, giving additional flexibility.

A low-level clock state (logic "0") allows information to be transferred to the master portion of the flip-flop through a "D" input. The master will continuously update itself to changing data as long as the clock is at a low level. When the clock goes to the high level, the master is disabled and the data transferred to the slave, thereby becoming available at the outputs. The thresholds of the master and slave portions of the flip-flop are internally offset to give a "raceless" flip-flop (i.e., the master is disabled before the slave is enabled, and vice versa). Thus the flip-flop operation is independent of the rise and fall times of the clock waveforms.

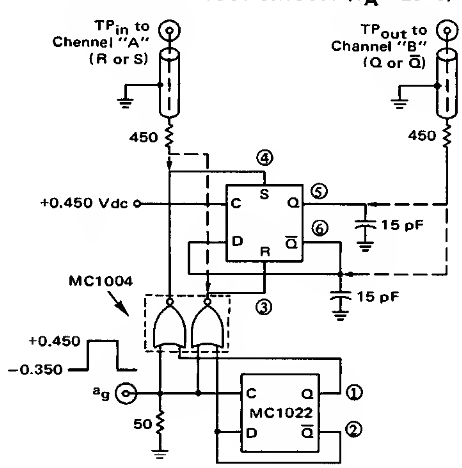
50 MHz SHIFT REGISTER



*Unused inputs should be returned to V_{EE}.

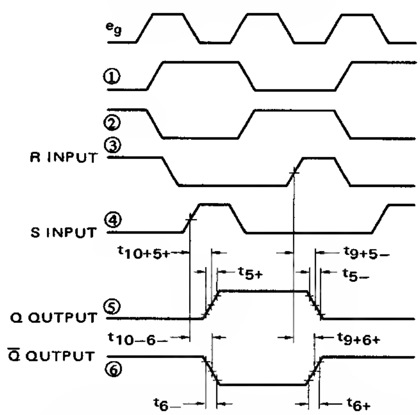
A "1" level on the Inhibit input may be used to stop the shifting of deta through the register. Perellel date may be brought into the register esynchronously since SET or RESET date internally inhibits the clock.

SWITCHING TIME TEST CIRCUIT (T_A = 25°C)



All Units V_{EE} = −4.0 Vdc, V_{CC} = +1.2 Vdc bypassed with 0.1 µF
Unused inputs returned to V_{EE}.

SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM



Switching time tast circuit and waveforms give method of test with input pulses on pins 9 or 10 and output pulsas on pins 5 and 6. Other tests specified and other combinations ere tested in same manner and will meet limits specified.

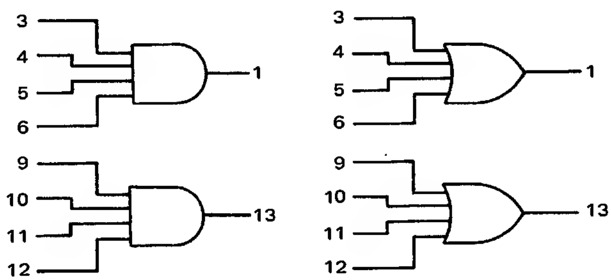
SATURATED LOGIC-TO-MECL
DUAL TRANSLATORS

MC1017
MC1217

Dual level translator intended for converting saturated logic levels to MECL signal levels. The translator provides the positive logic OR function.

POSITIVE LOGIC

NEGATIVE LOGIC

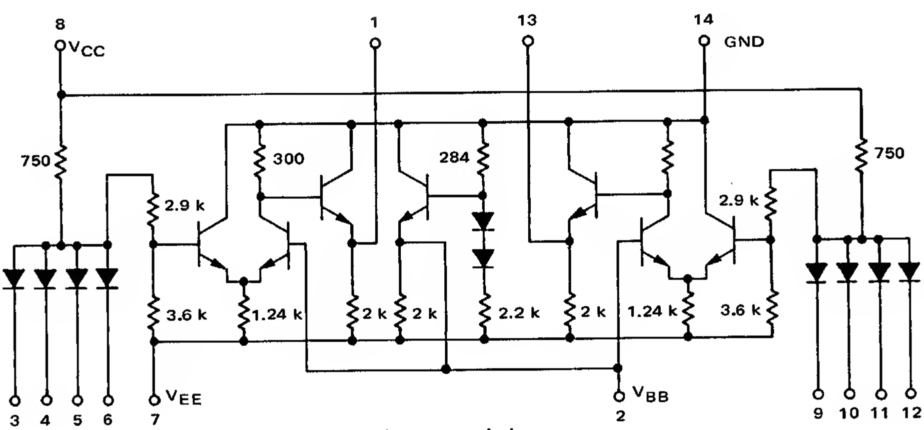


1 = 3 • 4 • 5 • 6

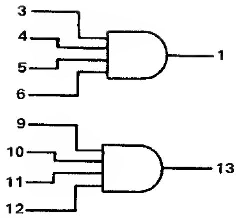
1 = 3 + 4 + 5 + 6

DC Input Loading Factor = 6 (DTL)
DC Output Loading Factor = 25 (MECL)
Power Dissipation = 150 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

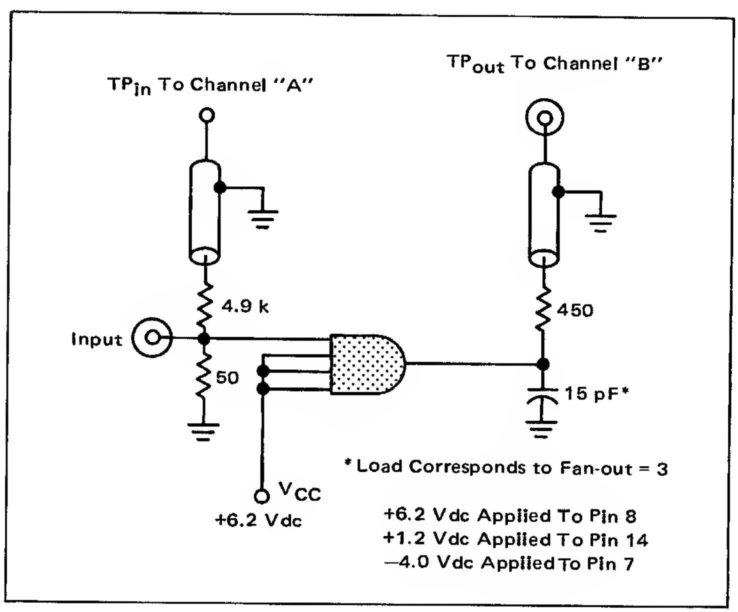
Test procedures are shown for only one translator.
The other translator is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1217 Test Limits −55°C Min	Max	+25°C Min	Max	+125°C Min	Max	Unit	MC1017 Test Limits 0°C Min	Max	+25°C Min	Max	+75°C Min	Max	Unit
Positive Supply Drain Current	I_C	8	-	-	-	4.0	-	-	mAdc	-	-	-	4.0	-	-	mAdc
Negative Supply Drain Current	I_E	7	-	-	-	24	-	-	mAdc	-	-	-	24	-	-	mAdc
Input Diode Reverse Current	I_R	3 4 5 6	- - - -	- - - -	- - - -	0.2 ↓	- - - -	2.0 ↓	µAdc ↓	- - - -	- - - -	- - - -	0.2 ↓	- - - -	2.0 ↓	µAdc ↓
Input Diode Forward Current	I_F	3 4 5 6	- - - -	- - - -	- - - -	7.5 ↓	- - - -	- - - -	mAdc ↓	- - - -	- - - -	- - - -	7.5 ↓	- - - -	- - - -	mAdc ↓
"OR" Logical "1" Output Voltage	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"OR" Logical "0" Output Voltage	V_{OL}	1 1 1 1	-1.890 ↓	-1.580 ↓	-1.800 ↓	-1.500 ↓	-1.720 ↓	-1.380 ↓	Vdc ↓	-1.830 ↓	-1.525 ↓	-1.800 ↓	-1.500 ↓	-1.760 ↓	-1.435 ↓	Vdc ↓
Bias Driver Output Voltage‡	V_{BB}†	2	-1.33	-1.19	-1.23	-1.09	-1.09	-0.95	Vdc	-1.28	-1.14	-1.23	-1.09	-1.19	-1.04	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{3+1+}	1	17	22	15	20	13	18	ns	16	21	15	20	14	19	ns
	t_{3-1-}	↓	13	18	15	20	19	25	↓	14	19	15	20	17	22	↓
Rise Time	t_{1+}	↓	7.0	10	7.0	10	8.0	12	↓	7.0	10	7.0	10	7.0	11	↓
Fall Time	t_{1-}	↓	7.0	10	7.0	10	8.0	12	↓	7.0	10	7.0	10	7.0	11	↓

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

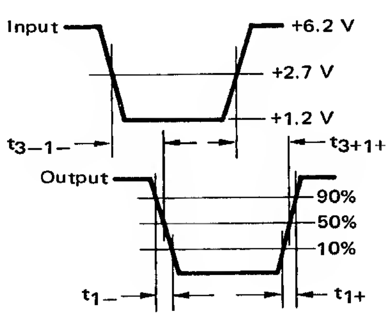
† V_{BB} limits apply from no load (0 mA) to full load (-1.0 mA).

SWITCHING TIME TEST CIRCUIT @ 25°C



	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% V_{IH}	V_{IL}	V_{max}	V_{CC}	V_{EE}	mAdc I_L
MC1217	−55°C	2.1	0.5	-	5.0	-5.2	-2.5
	+25°C	2.0	1.0	8.0	5.0	-5.2	-2.5
	+125°C	2.0	0.7	8.0	5.0	-5.2	-2.5
MC1017	0°C	2.0	0.85	-	5.0	-5.2	-2.5
	+25°C	1.9	1.00	8.0	5.0	-5.2	-2.5
	+75°C	1.8	0.85	8.0	5.0	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH}	V_{IL}	V_{max}	V_{CC}	V_{EE}	I_L	V_{CC} (Gnd)
Positive Supply Drain Current	I_C	8	-	-	-	8	7	-	14
Negative Supply Drain Current	I_E	7	-	-	-	8	7	-	14
Input Diode Reverse Current	I_R	3	-	-	3	-	-	-	4,5,6,14
		4	-	-	4	-	-	-	3,5,6,14
		5	-	-	5	-	-	-	3,4,6,14
		6	-	-	6	-	-	-	3,4,5,14
Input Diode Forward Current	I_F	3	-	-	-	8	7	-	3,14
		4	-	-	-	↓	↓	-	4,14
		5	-	-	-	↓	↓	-	5,14
		6	-	-	-	↓	↓	-	6,14
"OR" Logical "1" Output Voltage	V_{OH}‡	1	3,4,5,6	-	-	8	7	1	14
"OR" Logical "0" Output Voltage	V_{OL}	1	-	3	-	8	7	-	14
		1	-	4	-	↓	↓	-	↓
		1	-	5	-	↓	↓	-	↓
		1	-	6	-	↓	↓	-	↓
Bias Driver Output Voltage‡	V_{BB}†	2	-	-	-	8	7	2†	14
Switching Times			Pulse In	Pulse Out		(+6.2 V)	(−4.0 V)		(+1.2 V)
Propagation Delay	t_{3+1+}	1	1	3	-	8	7	-	14
	t_{3-1-}	↓	↓	↓	-	↓	↓	-	↓
Rise Time	t_{1+}	↓	↓	↓	-	↓	↓	-	↓
Fall Time	t_{1-}	↓	↓	↓	-	↓	↓	-	↓

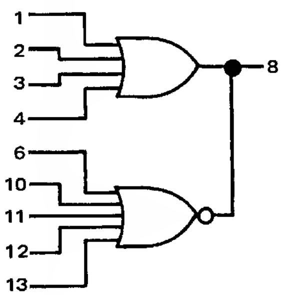


SWITCHING TIME WAVEFORMS

MC1018
MC1218

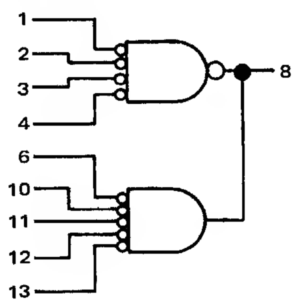
Level translator intended for converting MECL signal levels to saturated logic levels. The translator will provide the positive logic OR or logic NOR function by connecting the internal bias driver output to the corresponding inputs of the differential amplifier. i.e., when pin 4 is connected to the reference bias, pin 5, pins 6, 10, 11 12, and 13 become the inputs of a 5-input NOR gate. When pin 6 is connected to the reference bias, pin 5, pins 1, 2, 3, and 4 become the inputs of a 4-input OR gate.

POSITIVE LOGIC



$8 = 1+2+3+4$
or
$8 = \overline{6+10+11+12+13}$

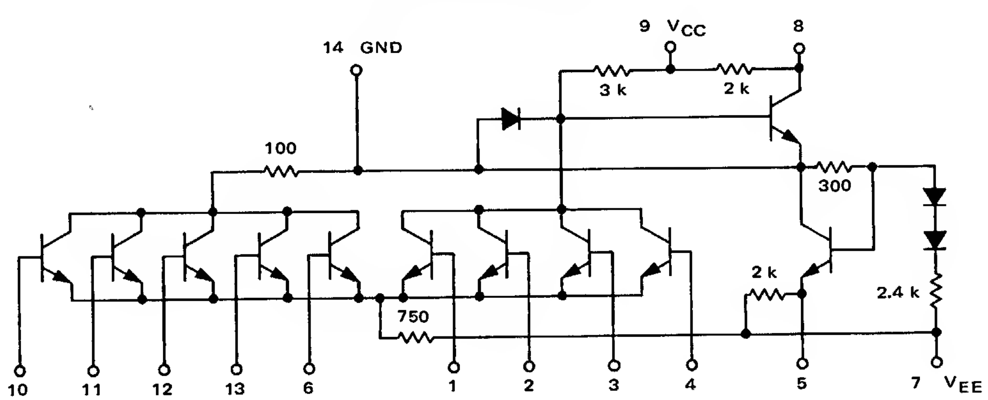
NEGATIVE LOGIC



$8 = \overline{1}\bullet\overline{2}\bullet\overline{3}\bullet\overline{4}$
or
$8 = \overline{6\bullet 10\bullet 11\bullet 12}$

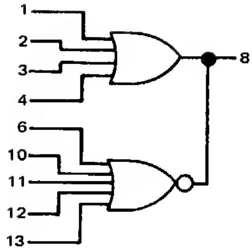
DC Input Loading Factor = 2 (MECL)
DC Output Loading Factor = 7 (DTL)
Power Dissipation = 55 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal.

MC1018, MC1218 (continued)



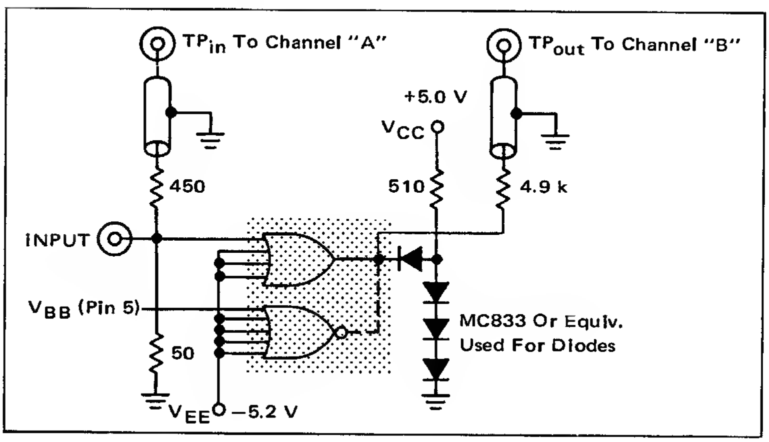
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1218 Test Limits							MC1018 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Positive Supply Drain Current	I_C	9	-	-	-	3.0	-	-	mAdc	-	-	-	3.0	-	-	mAdc
Negative Supply Drain Current	I_E	7	-	-	-	11.0	-	-	mAdc	-	-	-	11.0	-	-	mAdc
Input Current	I_{in}	1	-	-	-	200	-	-	μAdc	-	-	-	200	-	-	μAdc
		2	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		3	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		4	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		6	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		10	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		11	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		12	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		13	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
Input Leakage Current	I_R	1,2,3,4*	-	-	-	0.2	-	2.0	μAdc	-	-	-	0.2	-	2.0	μAdc
		6,10,11, 12,13*	-	-	-	0.2	-	2.0	μAdc	-	-	-	0.2	-	2.0	μAdc
Output Voltage High	V_{OH}	8 ↓	-	-	4.6 ↓	-	4.4 ↓	-	Vdc ↓	-	-	4.6 ↓	-	4.5 ↓	-	Vdc ↓
Output Voltage Low	V_{OL}	8 ↓	-	0.40 ↓	-	0.40 ↓	-	0.45 ↓	Vdc ↓	-	0.45 ↓	-	0.45 ↓	-	0.50 ↓	Vdc ↓
Bias Driver Output Voltage	V_{BB} ①	5	-1.33	-1.19	-1.23	-1.09	-1.09	-0.95	Vdc	-1.28	-1.14	-1.23	-1.09	-1.19	-1.04	Vdc
Output Short Circuit Current	I_{SC}	8	-	-4.0	-	-3.8	-	-3.6	mAdc	-	-3.9	-	-3.8	-	-3.6	mAdc
			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Switching Times	t_{1-8-}	8	19	25	19	25	19	25	ns	19	25	19	25	19	25	ns
	t_{1+8+}	↓	8.0	12	8.0	12	10	14	↓	8.0	12	8.0	12	9.0	13	↓
	t_{6-8+}	↓	8.0	12	8.0	12	10	14	↓	8.0	12	8.0	12	9.0	13	↓
	t_{6+8-}	↓	19	25	19	25	19	25	↓	12	25	19	25	19	25	↓

① V_{BB} is supplied from pin 5, and applies from no load (0 mA) to full load (-1.0 mAdc)

* Individually test each input using the pin connections shown.

SWITCHING TIME TEST CIRCUIT @ 25°C

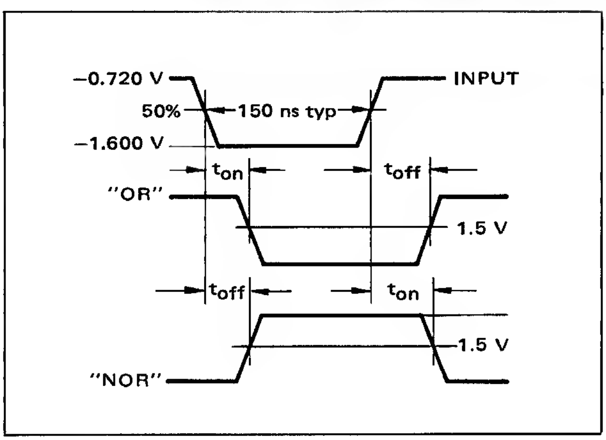


Circuit Shown For OR Configurations. Connect Pin 5 to 4 For NOR.

@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0%: $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{CC}	V_{EE}	V_{BB}	µA: I_{OH}	mAdc: I_{OL}	I_L
MC1218	−55°C	-5.2 to -1.405	-1.185 to -0.825	-	5.0	-5.2	1	-120	11.4	-1.0
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	5.0	-5.2	1	-120	12.0	-1.0
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	5.0	-5.2	1	-120	10.8	-1.0
MC1018	0°C	-5.2 to -1.350	-1.070 to -0.740	-	5.0	-5.2	1	-120	12.0	-1.0
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	5.0	-5.2	1	-120	12.0	-1.0
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	5.0	-5.2	1	-120	11.4	-1.0

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Characteristic	Pin Under Test	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{CC}	V_{EE}	V_{BB}	I_{OH}	I_{OL}	I_L	V_{CC} (Gnd)
Positive Supply Drain Current	9	-	-	-	9	1, 2, 3, 6, 7, 10, 11, 12, 13	4	-	-	-	14
Negative Supply Drain Current	7	-	-	-	9	1, 2, 3, 6, 7, 10, 11, 12, 13	4	-	-	-	14
Input Current	1	-	-	1	9	2, 3, 4, 7, 10, 11, 12, 13	6	-	-	-	14
	2	-	-	2	↓	1, 3, 4, 7, 10, 11, 12, 13	6	-	-	-	↓
	3	-	-	3	↓	1, 2, 4, 7, 10, 11, 12, 13	6	-	-	-	↓
	4	-	-	4	↓	1, 2, 3, 7, 10, 11, 12, 13	6	-	-	-	↓
	6	-	-	6	↓	1, 2, 3, 7, 10, 11, 12, 13	4	-	-	-	↓
	10	-	-	10	↓	1, 2, 3, 6, 7, 11, 12, 13	4	-	-	-	↓
	11	-	-	11	↓	1, 2, 3, 6, 7, 10, 12, 13	4	-	-	-	↓
	12	-	-	12	↓	1, 2, 3, 6, 7, 10, 11, 13	4	-	-	-	↓
	13	-	-	13	↓	1, 2, 3, 6, 7, 10, 11, 12	4	-	-	-	↓
Input Leakage Current	1, 2, 3, 4*	-	-	-	9	1, 2, 3, 4, 7, 10, 11, 12, 13	6	-	-	-	14
	6, 10, 11, 12, 13*	-	-	-	9	1, 2, 3, 6, 7, 10, 11, 12, 13	4	-	-	-	↓
Output Voltage High	8	6, 10, 11, 12, 13	-	-	9	1, 2, 3, 7	4	8	-	-	14
	↓	-	1	-	↓	2, 3, 4, 7, 10, 11, 12, 13	6	↓	-	-	↓
	↓	-	2	-	↓	1, 3, 4, 7, 10, 11, 12, 13	↓	↓	-	-	↓
	↓	-	3	-	↓	1, 2, 4, 7, 10, 11, 12, 13	↓	↓	-	-	↓
	↓	-	4	-	↓	1, 2, 3, 7, 10, 11, 12, 13	↓	↓	-	-	↓
Output Voltage Low	8	1, 2, 3, 4	-	-	9	7, 10, 11, 12, 13	6	-	8	-	14
	↓	-	6	-	↓	1, 2, 3, 7, 10, 11, 12, 13	4	-	↓	-	↓
	↓	-	10	-	↓	1, 2, 3, 6, 7, 11, 12, 13	↓	-	↓	-	↓
	↓	-	11	-	↓	1, 2, 3, 6, 7, 10, 12, 13	↓	-	↓	-	↓
	↓	-	12	-	↓	1, 2, 3, 6, 7, 10, 11, 13	↓	-	↓	-	↓
	↓	-	13	-	↓	1, 2, 3, 6, 7, 10, 11, 12	↓	-	↓	-	↓
Bias Driver Output Voltage	5	-	-	-	9	7	-	-	-	5	14
Output Short Circuit Current	8	-	-	4	9	1, 2, 3, 7, 10, 11, 12, 13	6	-	-	-	8, 14
		Pulse In	Pulse Out								
Switching Times	8	1	8	-	9	2, 3, 4, 7, 10, 11, 12, 13	6	-	-	-	14
	↓	1	↓	-	↓	2, 3, 4, 7, 10, 11, 12, 13	6	-	-	-	↓
	↓	6	↓	-	↓	1, 2, 3, 7, 10, 11, 12, 13	4	-	-	-	↓
	↓	6	↓	-	↓	1, 2, 3, 7, 10, 11, 12, 13	4	-	-	-	↓

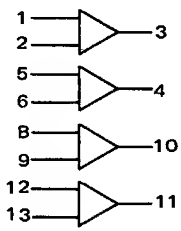


SWITCHING TIME WAVEFORMS

MC1020
MC1220

Four differential amplifiers with emitter follower outputs, intended for use as a comparator or for sensing differential signals over long lines. Each amplifier provides the OR or NOR logic function depending on which input is biased at a given reference voltage.

POSITIVE LOGIC

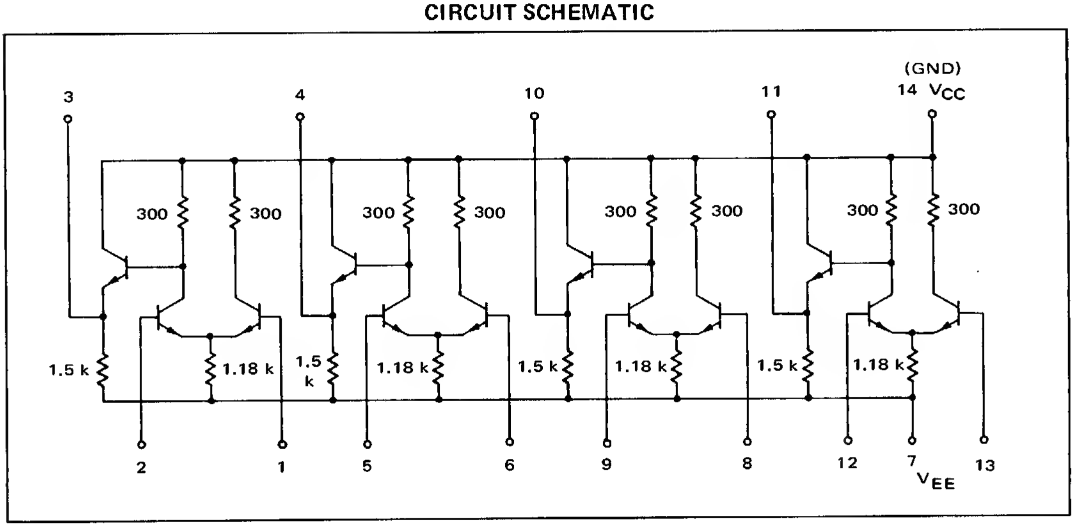


DC Input Loading Factor = 1
DC Output Loading Factor = 25

TRUTH TABLE

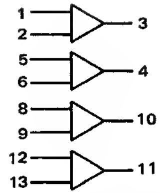
1	2	3	
6	5	4	
8	9	10	
13	12	11	
V_{BB}	H	L	NOR
V_{BB}	L	H	
H	V_{BB}	H	OR
L	V_{BB}	L	

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one line receiver.
The other line receivers are tested in the same manner.



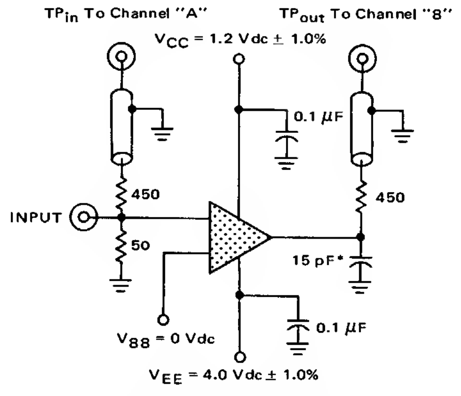
	@Test Temperature	TEST VOLTAGE/CURRENT VALUES — Vdc ±1.0% $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	V_{BB}	mAdc I_L
MC1220	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-1.270	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-1.025	-2.5
MC1020	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-1.210	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-1.115	-2.5

Characteristic	Symbol	Pin Under Test	MC1220 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1020 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	28	-	-	mAdc	-	-	-	28	-	-	mAdc
Input Current	I_{in}	1	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		2	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
Input Leakage Current	I_R	1	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
		2	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	3	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	3	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"OR" Logical "1" Output Voltage‡	V_{OH}‡	3	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"OR" Logical "0" Output Voltage	V_{OL}	3	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	·1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{1+3+}	3	4.0	7.0	4.0	7.0	5.0	8.0	ns	4.0	7.0	4.0	7.0	4.0	7.5	ns
	t_{1-3-}	↓	4.0	7.0	4.0	7.0	5.0	8.0	↓	4.0	7.0	4.0	7.0	4.0	7.5	↓
Rise Time (Fan-Out = 3)	t_{3+}	↓	4.0	7.0	4.0	7.0	5.0	8.0	↓	4.0	7.0	4.0	7.0	4.0	7.5	↓
Fall Time (Fan-Out = 3)	t_{3-}	↓	5.0	8.0	5.0	8.0	6.0	9.0	↓	5.0	8.0	5.0	8.0	5.0	8.5	↓

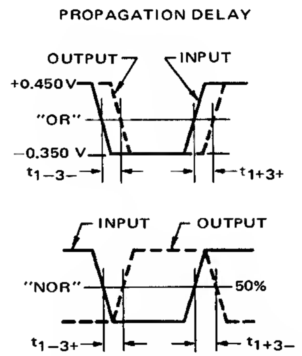
Characteristic	Symbol	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	V_{BB}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	-	-	-	2, 5, 7, 9, 12	1, 6, 8, 13	-	14
Input Current	I_{in}	-	-	1	5, 8, 7, 8, 9, 12, 13	2	-	14
		-	-	2	5, 6, 7, 8, 9, 12, 13	1	-	14
Input Leakage Current	I_R	-	-	-	1, 5, 6, 7, 8, 9, 12, 13	2	-	14
		-	-	-	2, 5, 6, 7, 8, 9, 12, 13	1	-	14
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	2	-	-	5, 6, 7, 8, 9, 12, 13	1	3	14
"NOR" Logical "0" Output Voltage	V_{OL}	-	2	-	5, 6, 7, 8, 9, 12, 13	1	-	14
"OR" Logical "1" Output Voltage‡	V_{OH}‡	-	1	-	5, 6, 7, 8, 9, 12, 13	2	-	14
"OR" Logical "0" Output Voltage	V_{OL}	1	-	-	5, 6, 7, 8, 9, 12, 13	2	-	14
Switching Times		Pulse In	Pulse Out		V_{EE} = −4.0 Vdc			(+1.2V)
Propagation Delay (Fan-Out = 3)	t_{1+3+}	1	3	-	5, 6, 7, 8, 9, 12, 13	2	-	14
	t_{1-3-}	↓	↓	-	↓	↓	-	↓
Rise Time (Fan-Out = 3)	t_{3+}	↓	↓	-	↓	↓	-	↓
Fall Time (Fan-Out = 3)	t_{3-}	↓	↓	-	↓	↓	-	↓

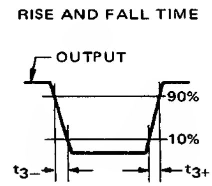
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



*Load Corresponds To Fan-out = 3





Input Pulse t_r and t_f = 5.0 ± 0.5 ns

Switching waveforms shown for pulse in on pin 1 and pulse out on pin 3, however all other input output combinations will meet the limits specified.

APPLICATIONS INFORMATION

The MC1020/MC1220 quad line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 1. Any MECL II gate with differential outputs may be used to drive the twisted pair line. The line is terminated in its characteristic impedance (around 100 ohms). A voltage divider is formed between the high-level gate output, the terminating resistor, and the pull-down resistor on the low-level gate output. The equivalent dc circuit is shown in Figure 2. The voltage swing across the terminating resistor (R_T) is typically ± 275 mV. Any input voltage swing in excess of 120 mV is adequate due to the voltage gain of the MC1020/MC1220. The output of the line receiver is the same as a standard MECL II gate. For worst-case pull-down resistors in the driving gate (1.5 k ohms ± 20%) and a $V_{OH\ min}$, the differential drop across an R_T of 100 ohms is ± 230 mV.

Very long lines may be used with excellent results. The only restriction on lead length (other than common mode noise) is series line resistance. The nominal voltage drop across R_T is actually shared with the series resistance of the twisted pair line. The resistance of # 22 AWG wire averages about 16 ohms per 1000 feet, while # 24 AWG wire averages about 26 ohms per 1000 feet. For very long lines, an additional voltage drop across R_T is easily obtained by paralleling additional pull-down resistors with those internal to the driver gate. For example, by paralleling a 1.5 k ohm resistor with each output, the voltage drop across R_T is effectively doubled.

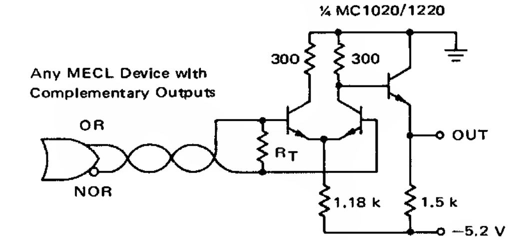
Extensive data have shown that a positive transient of 1.0 V or a negative transient of 1.8 V may be introduced on the twisted pair line before noise can propagate through another MECL device tied to the line receiver output. This method of data transmission is useful at frequencies to 50 MHz and results in the highest bandwidth — noise immunity product obtainable with digital logic. A twisted pair is recommended for clock distribution in high-speed systems since distribution skew time may be balanced out by adjusting line lengths. Propagation delay times are approximately 1.0 ns per eight inches of line.

In system design it is often convenient to organize information transfer with a data bus or "party-line" approach. In this application, one of many sources may "talk" to the common data line and multiple receivers may "listen". Figure 3 illustrates such a data bus utilizing MECL II gates as drivers and MC1020's as line receivers. Note that the line is unbalanced, but this will in turn allow all drivers to be ORed together. Bandwidth of data distribution is excellent. The techniqua may be used to 50 MHz at 25°C and to 40 MHz over the entire military temperature range. Noise immunity is also good due to the low impedance methods of transmission and the common mode rejection of the line receiver. The following results were obtained during an evaluation of the data bus shown in Figure 3 under worst-case conditions:

- Number of driver gates: 6
- Number of receivers: 8
- Line length: 24 feet
- Differential temperature from transmitter gate to receiver gate: 100°C
- Maximum operating frequency: 40 MHz
- Total terminating resistance: 45 ohms
- Differential power supply voltage from transmitter gate to receiver gate: ± 5.0%

The quad line receiver can also be used in many linear applications. The voltage gain is typically 7.0, with a bandwidth of approximately 70 MHz for each differential amplifier. The device makes an excellent FM limiter with minimal phase shift. By employing feedback, both selective band-pass amplifiers and notch frequency rejection amplifiers may be built. Figure 4 shows ¼ of the quad line receiver used as a parallel tuned-crystal oscillator that exhibits excellent stability.

FIGURE 1 - MECL LINE RECEIVER



$100\ \Omega < R_T < 130\ \Omega$

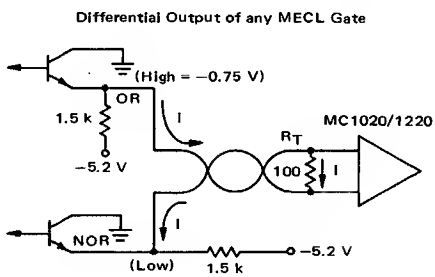
Driver worst-case $R_E = 1.8\ k\Omega$ @ $R_T = 100\ \Omega$ and $V_R = 230$ mV

Differential Gain = 15 dB or 6.0 V/V

Common Mode Gain = −18 dB or 0.12 V/V

Common Mode Voltage Rejection = 1.8 V (Negative pulse on lines)
1.0 V (Positive pulse on lines)

FIGURE 2 - LINE RECEIVER DC EQUIVALENT CIRCUIT



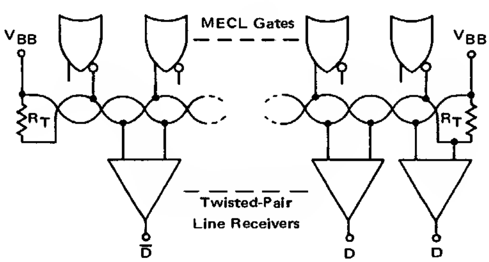
V_R = voltage drop across terminating resistor (R_T)

$$V_R = \frac{(5.2\ \text{V} - 0.75\ \text{V})\ (100\,\Omega)}{1.5\ \text{k}\Omega + 100\,\Omega}$$

$$= \frac{4.45\ (100)}{1.6\ \text{k}}$$

$$= 275\ \text{mV}$$

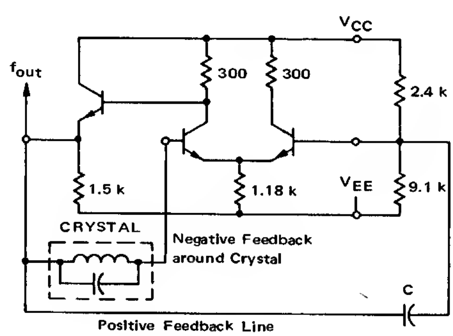
FIGURE 3 - DATA BUS DRIVING WITH MECL II



System Design Criteria

1. A total of two emitter pull-down resistors is recommended in the driver gates.
2. R_T should be Z_{out} of the twisted pair line ≈ 100 ohms
3. Either OR or NOR outputs may drive the line.
4. All driver gates are ORed together.
5. The line reciver output is Data or $\overline{\text{Data}}$ depending upon the input configuration.
6. V_{BB} should be able to source 7.0 mA or sink 8.0 mA total current.

FIGURE 4 - ¼ MC1020/1220 AS A PARALLEL-TUNED CRYSTAL OSCILLATOR



For further information see Application Note AN-417.

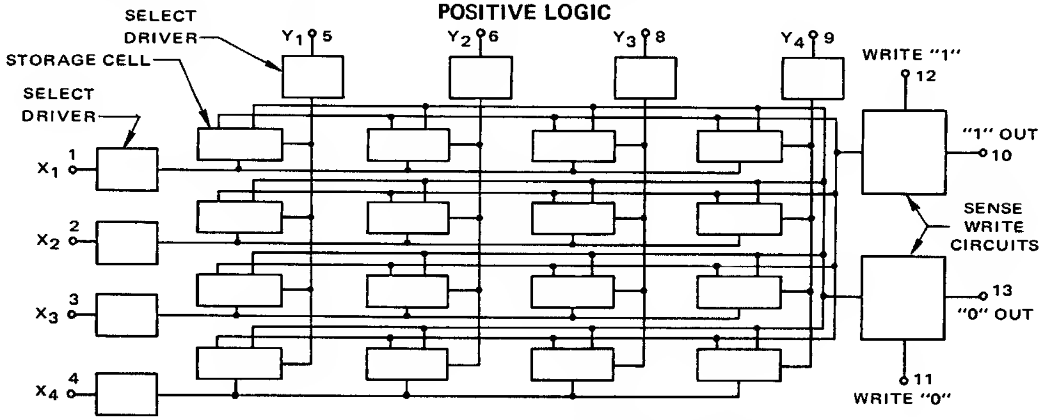
MC1036
MC1037

Designed for high-speed systems capable of cycle times as low as 50 ns. The memory is comprised of 16 multiple-emitter flip-flops, eight input emitter followers, and two nonsaturating complementary Sense/Write circuits. The flip-flops form an addressable 4 by 4 memory matrix that exhibits non-destructive readout for all 16 bits.

In operation a single bit is selected by applying a logical "1" to the coincident "X" and "Y" address lines. This gives a "read" condition where the sense amplifier outputs indicate the storage state of the selected bit. For example, if the bit store is a logical "1", the Sense "1" amplifier output will be a logical "1" and the Sense "0" amplifier will indicate the complement. With the desired "X" and "Y" lines at a logical "1", writing is accomplished by applying a logical "1" to the Write "1" input or to the Write "0" to obtain a bit store of a "1" or a "0" respectively.

The emitter-coupled sense amplifier outputs permit Wired-OR operation so that word expansion is easily obtained.

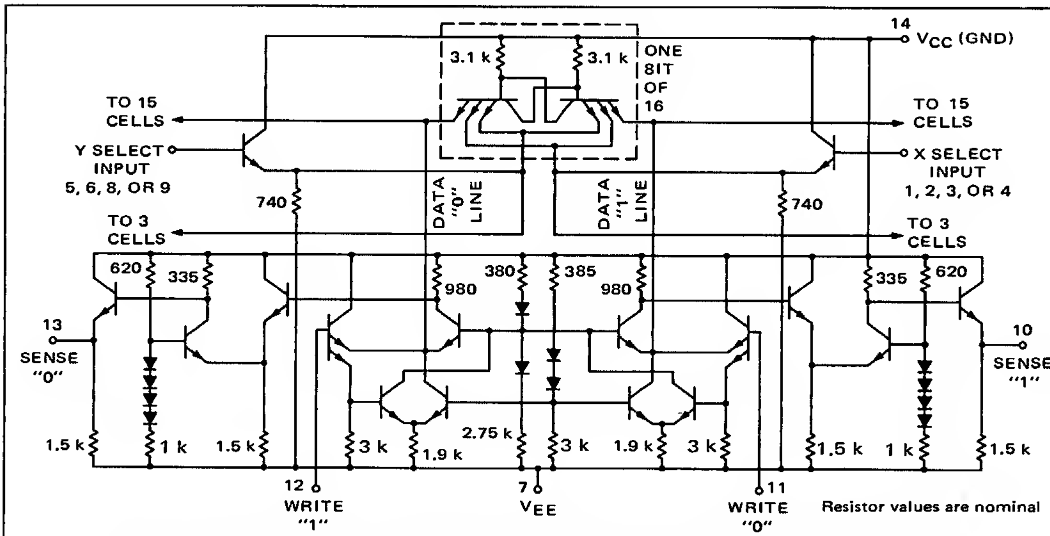
POSITIVE LOGIC



DC Input Loading Factor: X, Y = 2
Write = 0.5

DC Output Loading Factor = 5
Power Dissipation = 250 mW typical
Maximum Power Supply Variation = ±10%

CIRCUIT SCHEMATIC



MC1037 is identical to the MC1036 except the emitter follower output pulldown resistors are omitted. This allows large memory array design utilizing the Wired-OR feature, and minimum power dissipation.

ELECTRICAL CHARACTERISTICS

For MC1036 and MC1037: Test procedures are shown for only the X_1 input, for the X_1, $Y_{1,2,3,4}$ storage cells. To complete testing, sequence through remaining inputs, associated with remaining storage cells.

For MC1037 only: Outputs under test are connected to V_{EE} through 1.5 kΩ resistor.

@Test Temperature	TEST VOLTAGE/CURRENT VALUES				
	Vdc ± 1.0%				mAdc
	V_{IH}	$V_{IH\,max}$	V_{IL}	V_{EE}	I_L
0°C	-0.890	-	-1.525	-5.2	-0.5
+25°C	-0.850	-0.700	-1.500	-5.2	-0.5
+75°C	-0.790	-	-1.435	-5.2	-0.5

Characteristic	Symbol	Pin Under Test	MC1036, MC1037 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH}	$V_{IH\,max}$	V_{IL}	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	66	-	-	mAdc	1,5	-	2,3,4,6,8,9,11,12	7	-	14
Input Current	$2\,I_{in}$ $0.5\,I_{in}$ $0.5\,I_{in}$	1 11 12	- - -	- - -	- - -	200 50 50	- - -	- - -	μAdc ↓	- - -	1 11 12	2, 3, 4, 5, 6, 8, 9, 11, 12 1, 2, 3, 4, 5, 6, 8, 9, 12 1, 2, 3, 4, 5, 6, 8, 9, 11	7 ↓	- - -	14 ↓
Input Leakage Current	I_R	1 11 12	- - -	- - -	- - -	1.0 1.0 1.0	- - -	5.0 5.0 5.0	μAdc ↓	- - -	- - -	2, 3, 4, 5, 6, 8, 9, 11, 12 1, 2, 3, 4, 5, 6, 8, 9, 12 1, 2, 3, 4, 5, 6, 8, 9, 11	1, 7 7, 11 7, 12	- - -	14 ↓
Sense "1" Logical "1" Output Voltage‡	V_{OH}‡	10 ↓	-0.935 ↓	-0.740 ↓	-0.850 ↓	-0.700 ↓	-0.790 ↓	-0.615 ↓	Vdc ↓	1, 5, 12* 1, 6, 12* 1, 8, 12* 1, 9, 12*	- - - -	2, 3, 4, 6, 8, 9, 11 2, 3, 4, 5, 8, 9, 11 2, 3, 4, 5, 6, 9, 11 2, 3, 4, 5, 6, 8, 11	7 ↓	10 ↓	14 ↓
Sense "1" Logical "0" Output Voltage	V_{OL}	10 ↓	-1.830 ↓	-1.525 ↓	-1.800 ↓	-1.500 ↓	-1.760 ↓	-1.435 ↓	Vdc ↓	1, 5, 11* 1, 6, 11* 1, 8, 11* 1, 9, 11*	- - - -	2, 3, 4, 6, 8, 9, 12 2, 3, 4, 5, 8, 9, 12 2, 3, 4, 5, 6, 9, 12 2, 3, 4, 5, 6, 8, 12	7 ↓	- - - -	14 ↓
Sense "0" Logical "1" Output Voltage‡	V_{OH}‡	13 ↓	-0.935 ↓	-0.740 ↓	-0.850 ↓	-0.700 ↓	-0.790 ↓	-0.615 ↓	Vdc ↓	1, 5, 11* 1, 6, 11* 1, 8, 11* 1, 9, 11*	- - - -	2, 3, 4, 6, 8, 9, 12 2, 3, 4, 5, 8, 9, 12 2, 3, 4, 5, 6, 9, 12 2, 3, 4, 5, 6, 8, 12	7 ↓	13 ↓	14 ↓
Sense "0" Logical "0"	V_{OL}	13 ↓	-1.830 ↓	-1.525 ↓	-1.800 ↓	-1.500 ↓	-1.760 ↓	-1.435 ↓	Vdc ↓	1, 5, 12* 1, 6, 12* 1, 8, 12* 1, 9, 12*	- - - -	2, 3, 4, 6, 8, 9, 11 2, 3, 4, 5, 8, 9, 11 2, 3, 4, 5, 7, 9, 11 2, 3, 4, 5, 6, 8, 11	7 ↓	- - - -	14 ↓
Switching Times†			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out	V_{IL} + 1.2 Vdc	V_{EE} − 4.0 Vdc		(+1.2 Vdc)
Write Recovery	t_{12-13-}	13	22	30	22	30	25	35	ns	12	13	2, 3, 4, 6, 8, 9, 12	7	-	14
Output Turn-Off	t_{5+13+}	13	17	20	17	20	19	22	↓	1, 5	13	↓	↓	-	↓
Output Turn-On	t_{1-13-}	13	17	20	17	20	19	22		1, 5	13			-	

* V_{IH} applied momentarily to pin 11 or 12 as shown for 25 ns minimum.

† Pins 1 and 5 at V_{IH} + 1.2 Vdc.

‡ V_{OH} limits apply from no load (0 mA) to full load (-0.5 mA)

APPLICATIONS INFORMATION

A memory consisting of 16 words of N bits per word can be realized by connecting the selection lines of N 16-bit memories in parallel as shown in Figure 4. This results in a 4 by 4 selection matrix such that a word is selected by raising one X line and one Y line to the high state. The maximum value of N in this basic configuration is determined by the maximum fan-out of the gate used to drive the array. The recommended maximum N in this configuration is 12 (each input represents 2 dc loads) if MECL II gates are used to drive the X and Y selection lines and the wiring capacitance is a maximum of 3.0 pF per input.

The number of words can be increased by emitter ORing the outputs and/or using output gating. The emitter ORing technique is shown in Figure 5 for an N-bit by 16M-word memory. Memories 11, 21, . . ., N1 are MC1036's and the remaining units are MC1037's. In this way power dissipation is minimized and no external pulldown resistors are required. The maximum recommended M is 16 and the wiring capacitance should be a maximum of 3.0 pF per output.

A 256-word by 12-bit memory can be constructed without input or output gating (excluding selection gating) if the wiring capacitance can be kept reasonably small. The number of words and the number of bits per word can be increased by proper input and output gating.

FIGURE 1 – MINIMUM "WRITE" PULSE WIDTH versus TEMPERATURE

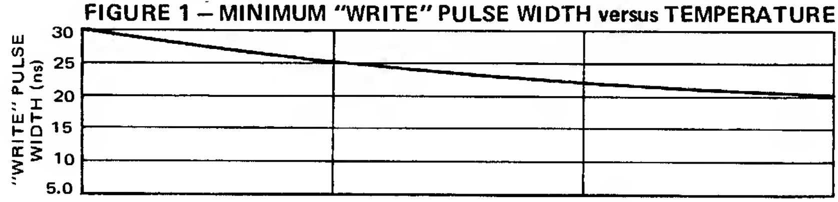


FIGURE 2 – TYPICAL "WRITE" RECOVERY TIME versus TEMPERATURE

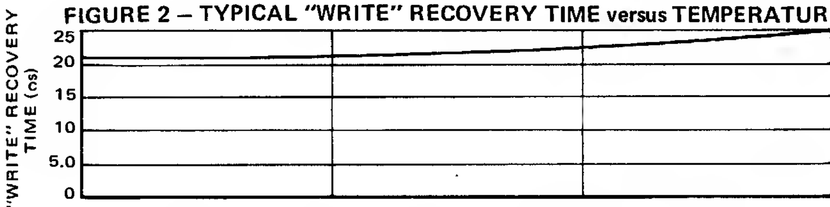


FIGURE 3 – TYPICAL "READ" TIME versus TEMPERATURE

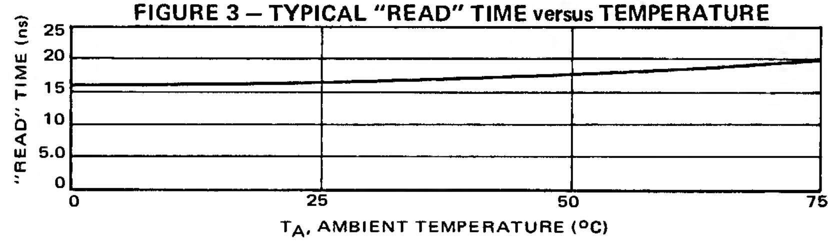


FIGURE 4 – 16-WORD BY N-BIT MEMORY

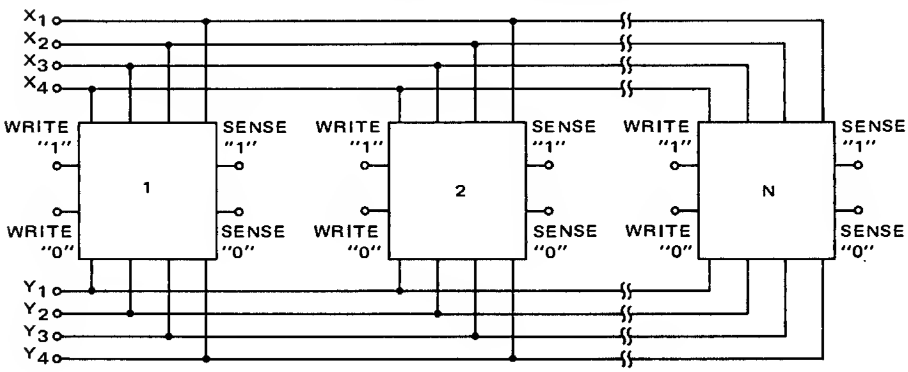
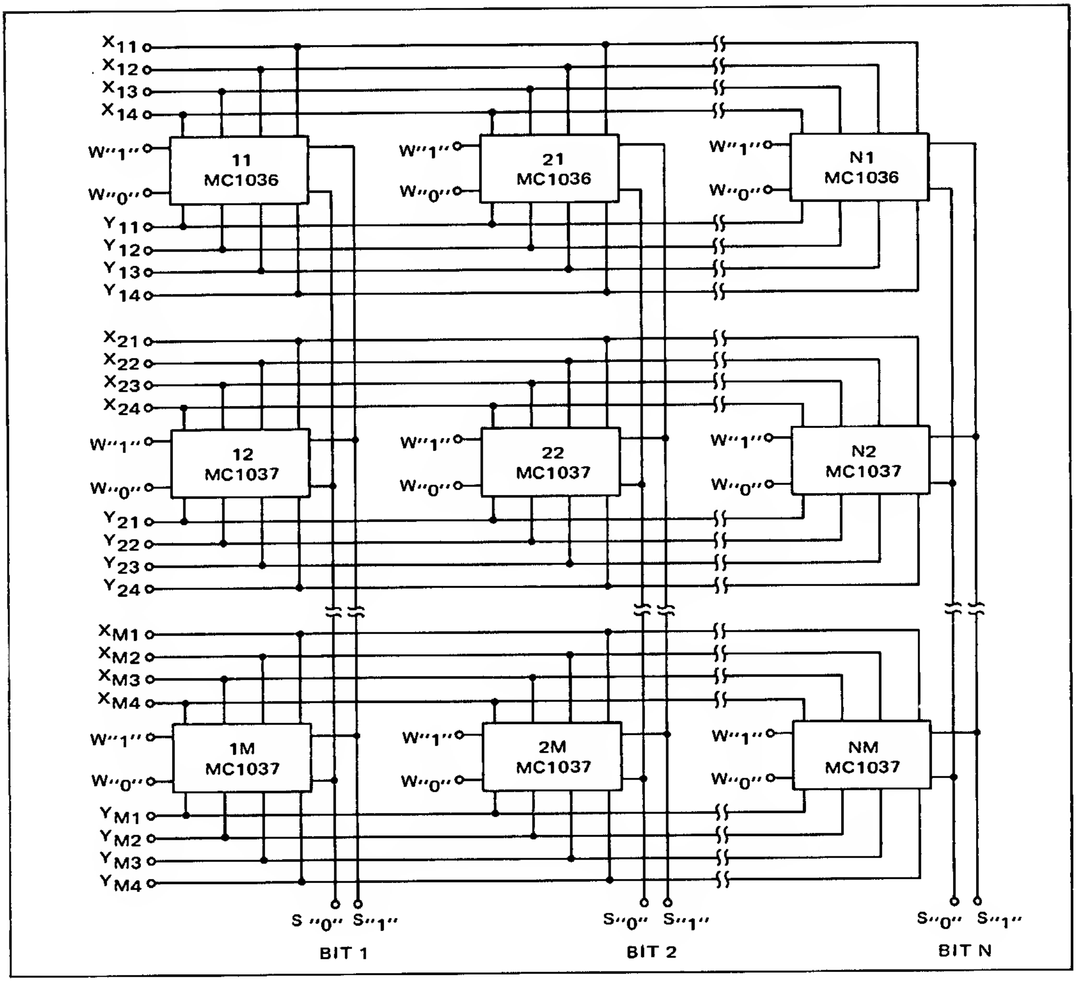
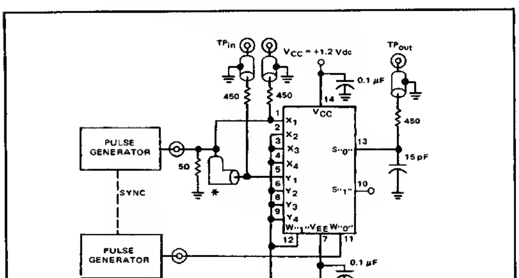


FIGURE 5 – INTERCONNECTION TECHNIQUE FOR N-BIT BY 16M-WORD MEMORY



SWITCHING TIME TEST CIRCUIT @ 25°C

(For t_{1-13-} and t_{5+13+})

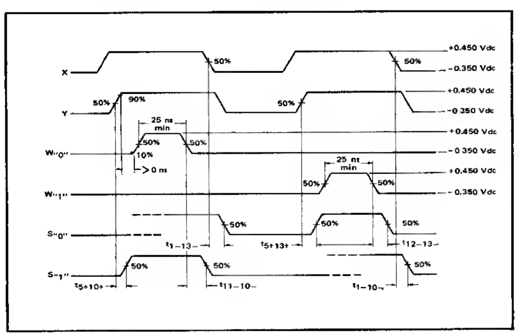


Input Pulse
$t_r = t_f = 5.0$ ns ±0.3 ns
f = 1.0 MHz typ

* Delay used to detect Y_1 going positive to S "0" going positive and X_1 going negative to S "0" going negative.

Other data input-output combinations are tested in the same manner and will meet limits specified. To measure from Write Inputs to corresponding outputs, alternating pulses must be applied to W "1" and W "0" while the select lines are high (see timing diagram).

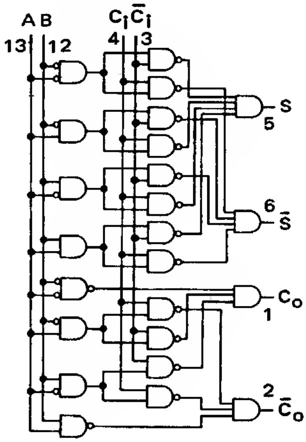
TIMING DIAGRAM @ T_A = 25°C



MC1019
MC1219

Provides the SUM, $\overline{\text{SUM}}$, CARRY, and $\overline{\text{CARRY}}$ functions while requiring only AUGEND (A) and ADDEND (B) inputs with CARRY IN and $\overline{\text{CARRY IN}}$.

POSITIVE LOGIC



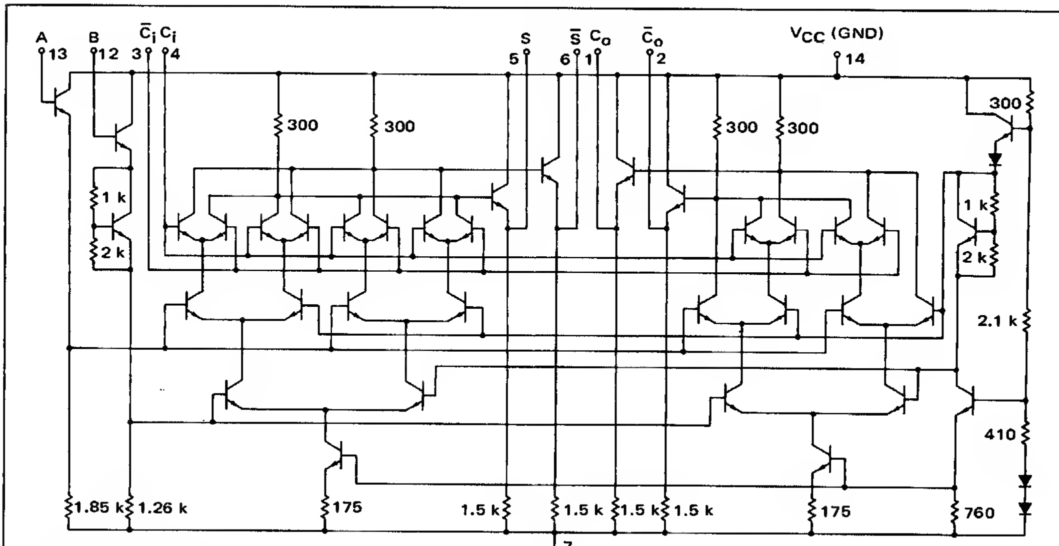
TRUTH TABLE

INPUT LOGIC LEVEL				OUTPUT LOGIC LEVEL			
A	B	C_i	$\bar{C}_i$	S	$\bar{S}$	C_o	$\bar{C}_o$
0	0	0	1	0	1	0	1
0	0	1	0	1	0	0	1
0	1	0	1	1	0	0	1
0	1	1	0	0	1	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	1	0
1	1	0	1	0	1	1	0
1	1	1	0	1	0	1	0

$S = ABC_i + A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i$
$\bar{S} = \bar{A}\bar{B}\bar{C}_i + AB\bar{C}_i + A\bar{B}C_i + \bar{A}BC_i$
$C_o = ABC_i + AB\bar{C}_i + A\bar{B}C_i + \bar{A}BC_i$
$\bar{C}_o = \bar{A}\bar{B}\bar{C}_i + \bar{A}\bar{B}C_i + \bar{A}B\bar{C}_i + A\bar{B}\bar{C}_i$

DC Input Loading Factor: A, B = 1
C_i, $\bar{C}_i$ = 2
DC Output Loading Factor = 25
Power Dissipation = 110 mW typical

CIRCUIT SCHEMATIC



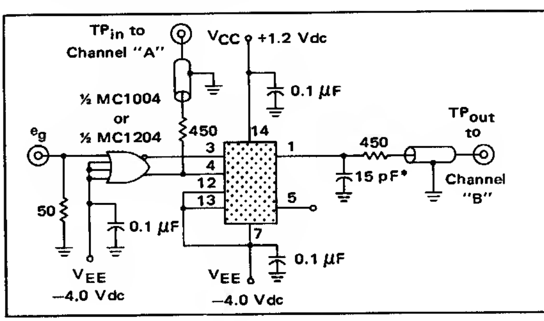
Resistor values are nominal.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1219 Test Limits							MC1019 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	30	-	-	mAdc	-	-	-	30	-	-	mAdc
Input Current	$2 I_{in}$	3	-	-	-	200	-	-	μAdc	-	-	-	200	-	-	μAdc
	$2 I_{in}$	4	-	-	-	200	-	-	↓	-	-	-	200	-	-	↓
	I_{in}	12	-	-	-	100	-	-	↓	-	-	-	100	-	-	↓
	I_{in}	13	-	-	-	100	-	-	↓	-	-	-	100	-	-	↓
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"SUM" Logical "1" Output Voltage‡	V_{OH}‡	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"SUM" Logical "0" Output Voltage	V_{OL}	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"CARRY" Logical "1" Output Voltage ‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"CARRY" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Addend Input Propagation Delay	t_{12-5+}	5	8.0	13.0	8.0	13.0	8.0	13.0	ns	8.0	13.0	8.0	13.0	8.0	13.0	ns
	t_{12+5-}	5	7.0	11.5	↓	12.0	10.0	16.0	↓	↓	12.0	↓	12.0	9.0	14.0	↓
	t_{12+1+}	1	8.0	12.0	↓	12.0	11.0	17.0	↓	↓	12.0	↓	12.0	↓	14.0	↓
	t_{12-1-}	1	9.0	14.5	9.0	14.5	10.0	15.0	↓	9.0	14.5	9.0	14.5	↓	14.5	↓
Rise Time	t_{5+}	5	8.0	13.0	9.0	14.0	9.0	14.0	↓	9.0	14.0	9.0	14.0	↓	14.0	↓
	t_{1+}	1	5.0	8.5	5.0	8.5	8.0	12.0	↓	5.0	8.5	5.0	8.5	7.0	10.0	↓
Fall Time	t_{5-}	5	↓	8.0	↓	8.5	7.0	11.5	↓	↓	8.5	↓	8.5	6.0	9.5	↓
	t_{1-}	1	↓	8.0	↓	8.0	7.0	10.0	↓	↓	8.0	↓	8.0	6.0	9.0	↓
Augend Input Propagation Delay	t_{13+5-}	5	6.0	8.5	6.0	8.5	7.0	10.5	ns	6.0	8.5	6.0	8.5	6.0	9.5	ns
	t_{13-5+}	↓	5.0	8.5	5.0	8.5	↓	11.0	↓	5.0	8.5	5.0	8.5	↓	9.0	↓
Rise Time	t_{5+}	↓	↓	↓	6.0	9.0	↓	11.0	↓	6.0	9.0	6.0	9.0	↓	9.5	↓
Fall Time	t_{5-}	↓	↓	↓	5.0	8.5	↓	11.0	↓	5.0	8.5	5.0	8.5	↓	9.5	↓
Carry Input Propagation Delay	t_{4-5+}	5	3.0	5.0	3.0	5.0	3.0	5.0	ns	3.0	5.0	3.0	5.0	3.0	5.0	ns
	t_{4+5-}	↓	4.0	7.5	4.0	7.5	6.0	10.0	↓	4.0	7.5	4.0	7.5	5.0	8.5	↓
Rise Time	t_{5+}	↓	5.0	8.0	6.0	8.5	7.0	10.5	↓	6.0	8.5	6.0	8.5	6.0	9.5	↓
Fall Time	t_{5-}	↓	5.0	8.0	5.0	8.5	7.0	11.0	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓

* Individually test each input using the pin connections shown. ‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA)

SWITCHING TIME TEST CIRCUIT @ 25°C



*Load corresponds to fan-out = 3.

Switching test circuit is shown for pulse in on pin 4 and pulse out on pin 1, however all other input–output combinations specified may be tested similarly according to the full subtractor truth table.

Input pulse t_r and t_f = 5.0 ± 0.5 ns

	@Test Temperature	TEST VOLTAGE/CURRENT VALUES				
		Vdc ±1.0%				mAdc
		$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L
MC1219	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1019	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	3, 4, 7, 12, 13	-	14
Input Current	$2\,I_{in}$	3	4, 13	-	3, 12	7	-	14
	$2\,I_{in}$	4	3, 12	-	4, 13	↓	-	↓
	I_{in}	12	3, 13	-	4, 12	↓	-	↓
	I_{in}	13	3, 12	-	4, 13	↓	-	↓
Input Leakage Current	I_R	Inputs*	-	-		3, 4, 7, 12, 13	-	14
"SUM" Logical "1" Output Voltage‡	V_{OH}‡	5	3, 12, 13	4	-	7	5	14
		↓	4, 13	3, 12	-	↓	↓	↓
		↓	4, 12	3, 13	-	↓	↓	↓
		↓	3	4, 12, 13	-	↓	↓	↓
"SUM" Logical "0" Output Voltage	V_{OL}	5	4, 12, 13	3	-	7	-	14
		↓	3, 13	4, 12	-	↓	-	↓
		↓	3, 12	4, 13	-	↓	-	↓
		↓	4	3, 12, 13	-	↓	-	↓
"CARRY" Logical "1" Output Voltage‡	V_{OH}‡	1	3, 13	4, 12	-	7	1	14
		↓	3, 12	4, 13	-	↓	↓	↓
		↓	4	3, 12, 13	-	↓	↓	↓
		↓	3	4, 12, 13	-	↓	↓	↓
"CARRY" Logical "0" Output Voltage	V_{OL}	1	4, 12, 13	3	-	7	-	14
		↓	3, 12, 13	4	-	↓	-	↓
		↓	4, 13	3, 12	-	↓	-	↓
		↓	4, 12	3, 13	-	↓	-	↓
Switching Times (Fan-out = 3)			Pulse In	Pulse Out		$V_{EE} = -4.0$ Vdc		(+1.2V)
Addend Input Propagation Delay	t_{12-5+}	5	12	5	-	7	-	14
	t_{12+5-}	5	↓	5	-	↓	-	↓
	t_{12+1+}	1	↓	1	-	↓	-	↓
	t_{12-1-}	1	↓	1	-	↓	-	↓
Rise Time	t_{5+}	5	↓	5	-	↓	-	↓
	t_{1+}	1	↓	1	-	↓	-	↓
Fall Time	t_{5-}	5	↓	5	-	↓	-	↓
	t_{1-}	1	↓	1	-	↓	-	↓
Augend Input Propagation Delay	t_{13+5-}	5	13	5	-	7	-	14
	t_{13-5+}	↓	↓	↓	-	↓	-	↓
Rise Time	t_{5+}	↓	↓	↓	-	↓	-	↓
Fall Time	t_{5-}	↓	↓	↓	-	↓	-	↓
Carry Input Propagation Delay	t_{4-5+}	5	4	5	-	7	-	14
	t_{4+5-}	↓	↓	↓	-	↓	-	↓
Rise Time	t_{5+}	↓	↓	↓	-	↓	-	↓
Fall Time	t_{5-}	↓	↓	↓	-	↓	-	↓

SWITCHING TIME WAVEFORMS

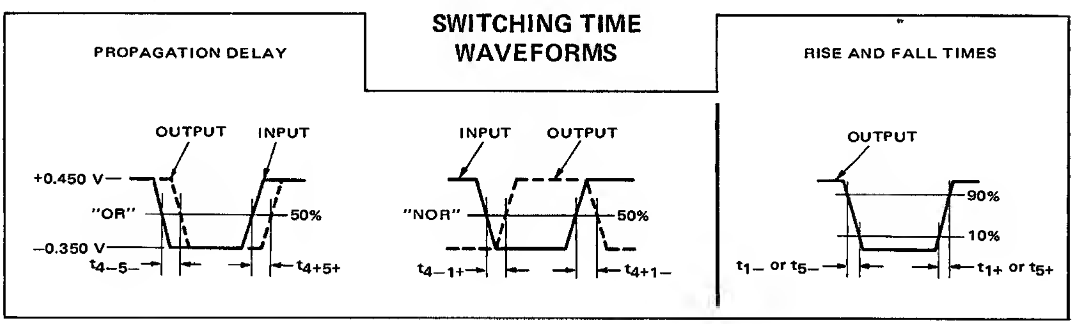
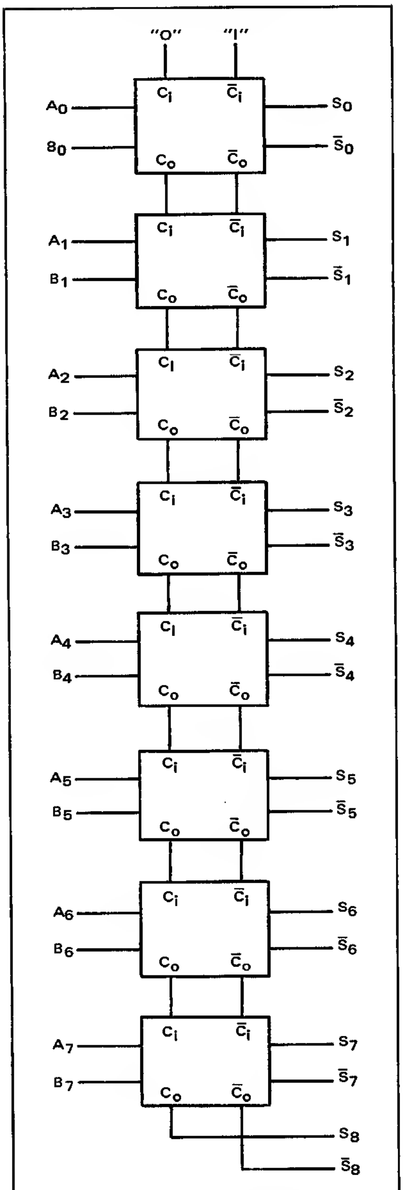


FIGURE 1 - 8 BIT RIPPLE-THROUGH ADDER



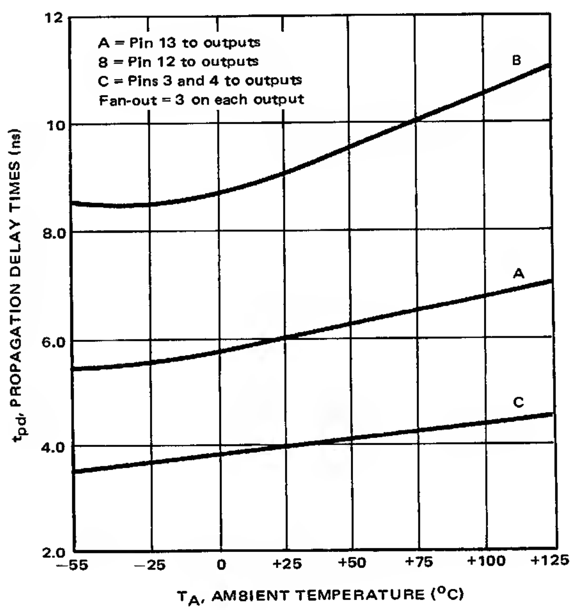
Total Add Time for 8 stage ripple through is typically 37 ns.

APPLICATIONS INFORMATION

The MC1019/MC1219 full adder exhibits an average propagation delay time of 5.0 ns per stage in a system employing ripple Carry. This device permits practical ripple-through adders as shown in Figure 1, as well as ripple-through multipliers.

The schematic of the full adder illustrates the techniques employed to obtain the necessary logic equations. A compensated current source drives a transistor "tree" with three levels of branching. The B input is translated negative two levels, to switch current between either the left or right branch of the tree. The A input is translated negative one level to switch current at the second level of branching. The Carry inputs switch current through the third level of branching. Depending upon the eight possible combinations of inputs, one specific branch in the Sum generating tree will be carrying current. Thus the proper output state is determined. The Carry generating tree operates in the same manner. This series gating technique results in the best speed-power product obtainable with bipolar technology. Typical propagation delay times from the inputs to outputs are shown in Figure 2.

FIGURE 2 - TYPICAL PROPAGATION DELAY TIMES

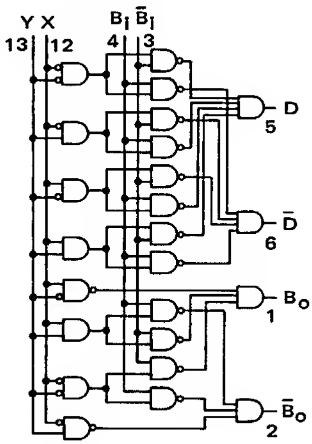


FULL SUBTRACTORS

MC1021
MC1221

Provides the DIFFERENCE, $\overline{\text{DIFFERENCE}}$, BORROW OUT, and $\overline{\text{BORROW OUT}}$ functions while requiring only MINUEND (X) and SUBTRAHEND (Y) inputs with BORROW IN and $\overline{\text{BORROW IN}}$.

POSITIVE LOGIC



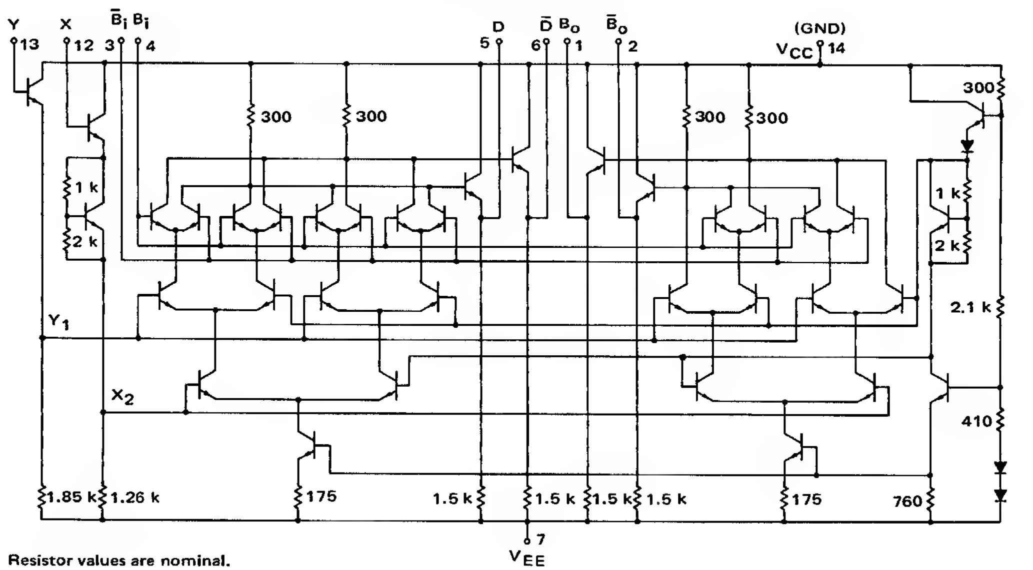
$$D = YXB_i + Y\overline{X}\overline{B}_i + \overline{Y}X\overline{B}_i + \overline{Y}\overline{X}B_i$$
$$\overline{D} = \overline{Y}\overline{X}\overline{B}_i + YX\overline{B}_i + Y\overline{X}B_i + \overline{Y}XB_i$$
$$B_o = \overline{Y}\overline{X}B_i + Y\overline{X}\overline{B}_i + Y\overline{X}B_i + YXB_i$$
$$\overline{B}_o = \overline{Y}\overline{X}\overline{B}_i + \overline{Y}X\overline{B}_i + \overline{Y}XB_i + YX\overline{B}_i$$

DC Input Loading Factor: X, Y = 1 B_i, $\overline{B}_i$ = 2
DC Output Loading Factor = 25
Power Dissipation = 110 mW typical

TRUTH TABLE

INPUT LOGIC LEVEL				OUTPUT LOGIC LEVEL			
X	Y	B_i	$\overline{B}_i$	D	$\overline{D}$	B_o	$\overline{B}_o$
0	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0
0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	0	1
1	1	0	1	0	1	0	1
1	1	1	0	1	0	1	0

CIRCUIT SCHEMATIC



Resistor values are nominal.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1221 Test Limits							MC1021 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	30	-	-	mAdc	-	-	-	30	-	-	mAdc
Input Current	$2\ I_{in}$	3	-	-	-	200	-	-	μAdc	-	-	-	200	-	-	μAdc
	$2\ I_{in}$	4	-	-	-	200	-	-	↓	-	-	-	200	-	-	↓
	I_{in}	12	-	-	-	100	-	-	↓	-	-	-	100	-	-	↓
	I_{in}	13	-	-	-	100	-	-	↓	-	-	-	100	-	-	↓
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"DIFFERENCE" Logical "1" Output Voltage‡	V_{OH}‡	5 ↓	-0.990 ↓	-0.825 ↓	-0.850 ↓	-0.700 ↓	-0.700 ↓	-0.530 ↓	Vdc ↓	-0.895 ↓	-0.740 ↓	-0.850 ↓	-0.700 ↓	-0.775 ↓	-0.615 ↓	Vdc ↓
"DIFFERENCE" Logical "0" Output Voltage	V_{OL}	5 ↓	-1.890 ↓	-1.580 ↓	-1.800 ↓	-1.500 ↓	-1.720 ↓	-1.380 ↓	Vdc ↓	-1.830 ↓	-1.525 ↓	-1.800 ↓	-1.500 ↓	-1.760 ↓	-1.435 ↓	Vdc ↓
"BORROW" Logical "1" Output Voltage‡	V_{OH}‡	1 ↓	-0.990 ↓	-0.825 ↓	-0.850 ↓	-0.700 ↓	-0.700 ↓	-0.530 ↓	Vdc ↓	-0.895 ↓	-0.740 ↓	-0.850 ↓	-0.700 ↓	-0.775 ↓	-0.615 ↓	Vdc ↓
"BORROW" Logical "0" Output Voltage	V_{OL}	1 ↓	-1.890 ↓	-1.580 ↓	-1.800 ↓	-1.500 ↓	-1.720 ↓	-1.380 ↓	Vdc ↓	-1.830 ↓	-1.525 ↓	-1.800 ↓	-1.500 ↓	-1.760 ↓	-1.435 ↓	Vdc ↓
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Minuend Input Propagation Delay	t_{12-5+}	5	9.0	14	8.0	13	9.0	14.5	ns	8.0	13	8.0	13	8.0	13	ns
	t_{12+5-}	5	8.0	13	8.0	13.5	11	17	↓	8.0	13.5	8.0	13.5	9.0	15	↓
	t_{12-1+}	1	↓	14	7.0	12.5	9.0	14.5	↓	7.0	12.5	7.0	12.5	8.0	13	↓
	t_{12+1-}	1	↓	13.5	8.0	13.5	11	17	↓	8.0	13.5	8.0	13.5	9.0	15	↓
Rise Time	t_{5+}	5	↓	13	9.0	14	10	14	↓	9.0	14	9.0	14	9.0	14	↓
	t_{1+}	1	↓	13	7.0	12	9.0	14	↓	7.0	12	7.0	12	8.0	13	↓
Fall Time	t_{5-}	5	5.0	8.0	5.0	8.5	7.0	11.5	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
	t_{1-}	1	5.0	8.0	5.0	8.0	7.0	11.0	↓	5.0	8.0	5.0	8.0	6.0	9.0	↓
Subtrahend Input Propagation Delay	t_{13+5-}	5	5.0	8.5	5.0	8.5	7.0	11	ns	5.0	8.5	5.0	8.5	6.0	9.5	ns
	t_{13-5+}	↓	6.0	9.0	5.0	8.5	7.0	11.5	↓	5.0	8.5	5.0	8.5	6.0	9.0	↓
Rise Time	t_{5+}	↓	5.0	8.5	6.0	9.0	8.0	11	↓	6.0	9.0	6.0	9.0	7.0	9.5	↓
Fall Time	t_{5-}	↓	5.0	8.5	5.0	8.5	7.0	11	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
Borrow Input Propagation Delay	t_{4-5+}	5	3.0	5.5	3.0	5.0	4.0	6.0	ns	3.0	5.0	3.0	5.0	3.0	5.0	ns
	t_{4+5-}	↓	4.0	7.5	4.0	7.5	6.0	10	↓	4.0	7.5	4.0	7.5	5.0	8.5	↓
Rise Time	t_{5+}	↓	5.0	8.0	6.0	8.5	8.0	10.5	↓	6.0	8.5	6.0	8.5	7.0	10	↓
Fall Time	t_{5-}	↓	5.0	8.0	5.0	8.5	7.0	11	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓

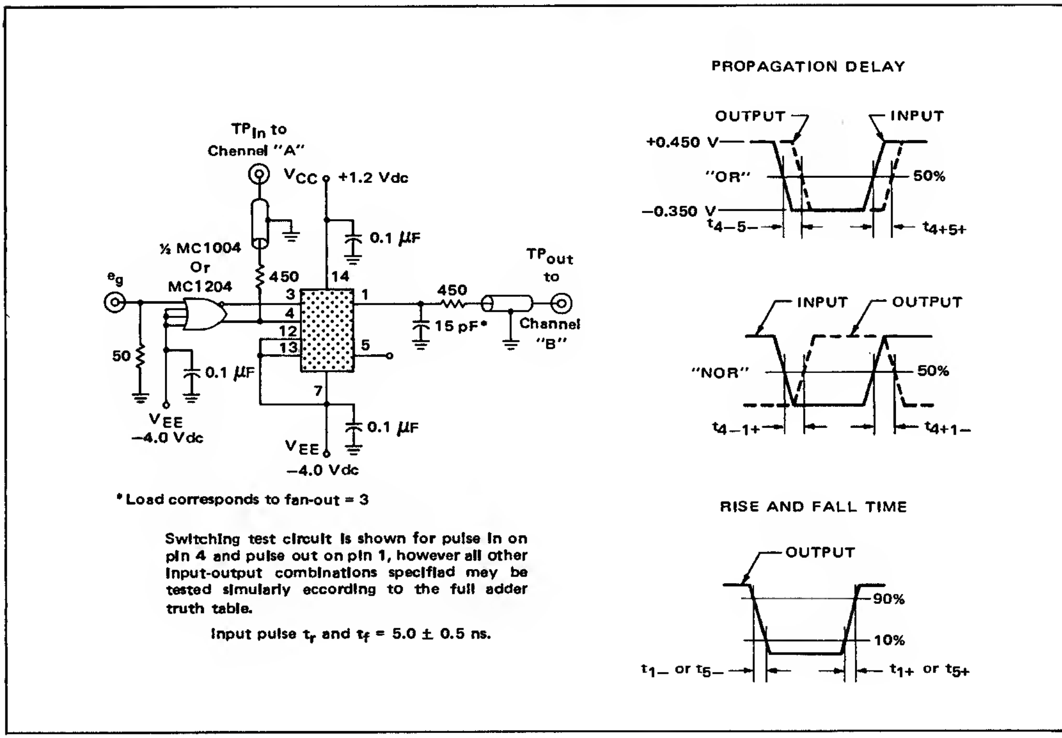
* Individually test each input using the pin connections shown.

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

	@Test Temperature	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L
		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0%				mAdc
MC1221	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
MC1221	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
MC1221	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1021	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
MC1021	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
MC1021	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
			TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					
Power Supply Drain Current	I_E	7	-	-	-	3, 4, 7, 12, 13	-	14
Input Current	$2\,I_{in}$	3	4, 13		3, 12	7	-	14
	$2\,I_{in}$	4	3, 12		4, 13	↓	-	↓
	I_{in}	12	3, 13		4, 12	↓	-	↓
	I_{in}	13	3, 12		4, 13	↓	-	↓
Input Leakage Current	I_R	Inputs*	-	-	-	3, 4, 7, 12, 13	-	14
"DIFFERENCE" Logical "1" Output Voltage‡	V_{OH}‡	5	3, 12, 13	4	-	7	5	14
		↓	4, 13	3, 12	-	↓	↓	↓
		↓	4, 12	3, 13	-	↓	↓	↓
		↓	3	4, 12, 13	-	↓	↓	↓
"DIFFERENCE" Logical "0" Output Voltage	V_{OL}	5	4, 12, 13	3	-	7	-	14
		↓	3, 13	4, 12	-	↓	-	↓
		↓	3, 12	4, 13	-	↓	-	↓
		↓	4	3, 12, 13	-	↓	-	↓
"BORROW" Logical "1" Output Voltage‡	V_{OH}‡	1	3, 12, 13	4	-	7	1	14
		↓	3, 12	4, 13	-	↓	↓	↓
		↓	4, 12	3, 13	-	↓	↓	↓
		↓	3	4, 12, 13	-	↓	↓	↓
"BORROW" Logical "0" Output Voltage	V_{OL}	1	4, 12, 13	3	-	7	-	14
		↓	4, 13	3, 12	-	↓	-	↓
		↓	3, 13	4, 12	-	↓	-	↓
		↓	4	3, 12, 13	-	↓	-	↓
Switching Times			Pulse In	Pulse Out		$V_{EE} = -4.0$ Vdc		+1.2V
Minuend Input Propagation Delay	t_{12-5+}	5	12	5	-	7	-	14
	t_{12+5-}	5	↓	5	-	↓	-	↓
	t_{12-1+}	1	↓	1	-	↓	-	↓
	t_{12+1-}	1	↓	1	-	↓	-	↓
Rise Time	t_{5+}	5	↓	5	-	↓	-	↓
	t_{1+}	1	↓	1	-	↓	-	↓
Fall Time	t_{5-}	5	↓	5	-	↓	-	↓
	t_{1-}	1	↓	1	-	↓	-	↓
Subtrahend Input Propagation Delay	t_{13+5-}	5	13	5	-	7	-	14
	t_{13-5+}	↓	↓	↓	-	↓	-	↓
Rise Time	t_{5+}	↓	↓	↓	-	↓	-	↓
Fall Time	t_{5-}	↓	↓	↓	-	↓	-	↓
Borrow Input Propagation Delay	t_{4-5+}	5	4	5	-	7	-	14
	t_{4+5-}	↓	↓	↓	-	↓	-	↓
Rise Time	t_{5+}	↓	↓	↓	-	↓	-	↓
Fall Time	t_{5-}	↓	↓	↓	-	↓	-	↓

SWITCHING TIME TEST CIRCUIT
AND WAVEFORMS @ 25°C



*Load corresponds to fan-out = 3

Switching test circuit is shown for pulse in on pin 4 and pulse out on pin 1, however all other input-output combinations specified may be tested similarly according to the full adder truth table.

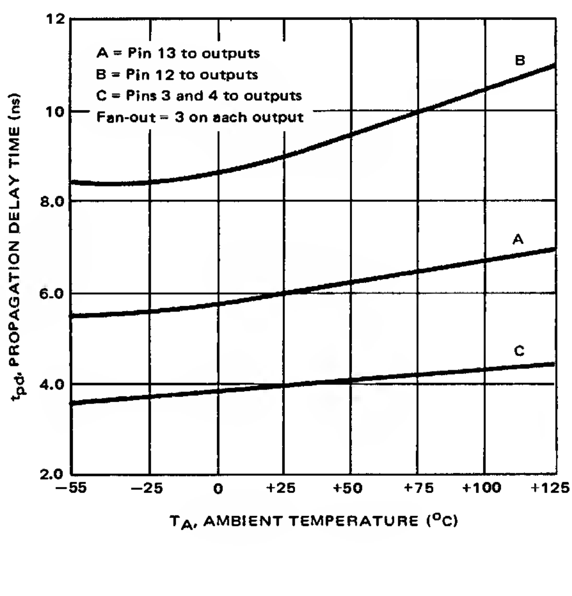
Input pulse t_r and t_f = 5.0 ± 0.5 ns.

APPLICATIONS INFORMATION

The MC1021/MC1221 full subtractor is identical to the full adder except for the interconnection metalization. It exhibits an average propagation delay time of 5.0 ns per stage in a system employing ripple Borrow. This device permits building of ripple-through dividers.

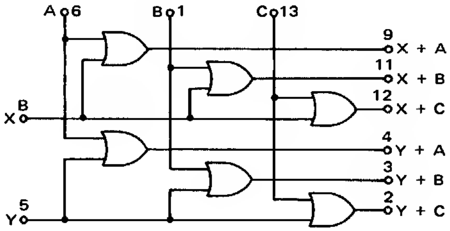
The schematic of the full subtractor illustrates the techniques employed to obtain the necessary logic equations. A compensated current source drives a transistor "tree" with three levels of branching. The X input is translated negative two levels, to switch current between either the left or right brench of the tree. The Y input is translated negative one level to switch current at the second level of branching. Depending upon the eight possible combinations of inputs, one specific branch level in the Difference genereting tree will be carrying current. Thus the proper output state is determined. The Borrow generating tree operetes in the same manner. This series gating technique results in the best speed-power product obtainable with bipolar technology. Typical propagation delay times from the inputs to outputs are shown.

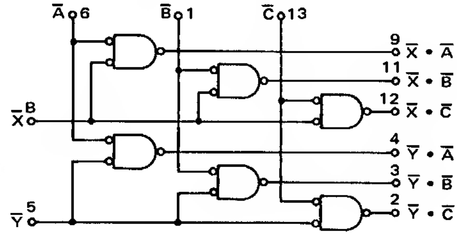
TYPICAL PROPAGATION DELAY TIMES



MC1029
MC1229

A 2 X 3 array of 2-input OR gates, designed primarily for the handling of data in a digital system.



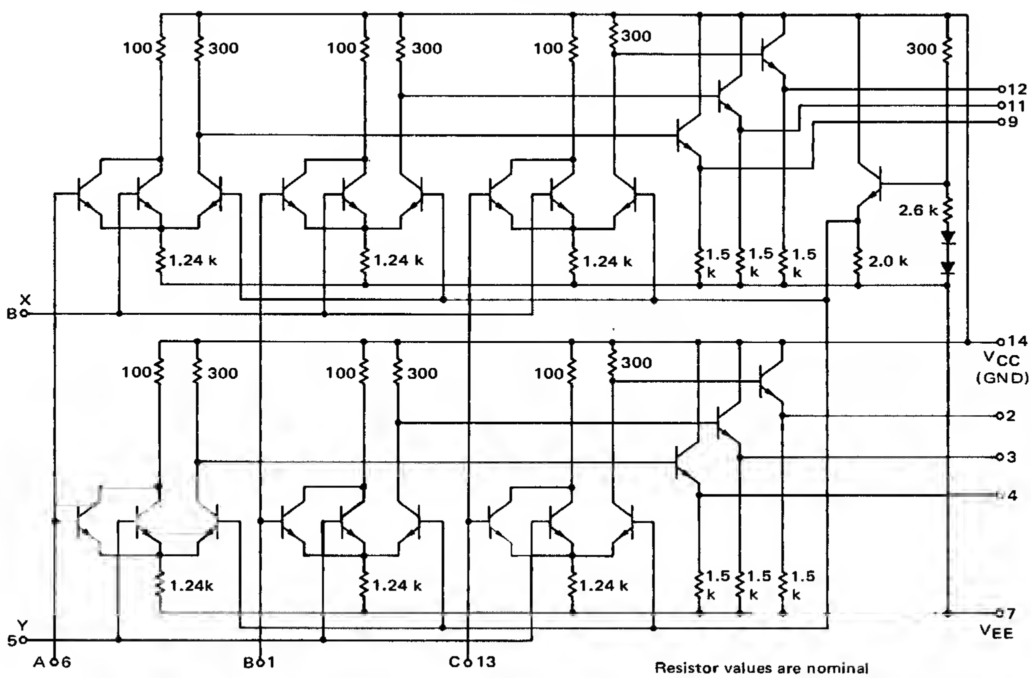


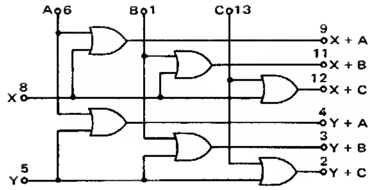
DC Input Loading Factors: X, Y = 3; A, B, C = 2
DC Output Loading Factor = 25
Power Dissipation = 160 mW typical

TRUTH TABLE (POSITIVE LOGIC)

					PIN NUMBER					
X	Y	A	B	C	9	11	12	4	3	2
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1	0	0	1
0	0	0	1	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0	1	0	0
0	1	0	0	0	0	0	0	1	1	1
1	0	0	0	0	1	1	1	0	0	0

CIRCUIT SCHEMATIC



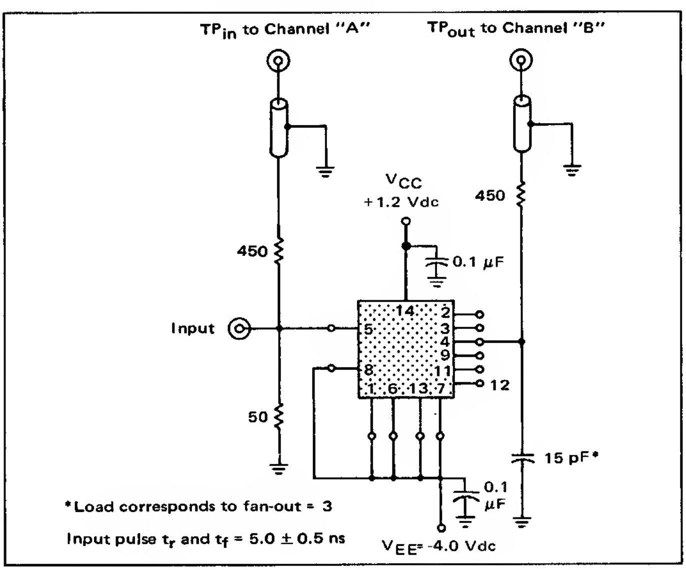


ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1229 Test Limits							MC1029 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	45	-	-	mAdc
Input Current	I_{in}	5	-	-	-	300	-	-	μAdc	-	-	-	300	-	-	μAdc
		8	-	-	-	300	-	-		-	-	-	300	-	-	
		1	-	-	-	200	-	-		-	-	-	200	-	-	
		6	-	-	-	200	-	-		-	-	-	200	-	-	
		13	-	-	-	200	-	-	↓	-	-	-	200	-	-	↓
Input Leakage Current	I_R	5, 8*	-	-	-	0.6	-	3.0	μAdc	-	-	-	0.6	-	3.0	μAdc
		1, 6, 13*	-	-	-	0.4	-	2.0	μAdc	-	-	-	0.4	-	2.0	μAdc
Logical "1" Output Voltage	V_{OH}‡	3, 11†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		4, 9†	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
		2, 12†														
		2, 3, 4†														
		9, 11, 12†														
Logical "0" Output Voltage	V_{OL}	3, 11†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		4, 9†	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
		2, 12†														
		2, 3, 4†														
		9, 11, 12†														
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{5+4+}	4	4.0	7.5	4.0	7.5	6.0	9.0	ns	4.0	7.5	4.0	7.5	5.0	8.0	ns
	t_{5-4-}	↓	4.0	7.5	4.0	7.5	6.0	9.0	↓	4.0	7.5	4.0	7.5	5.0	8.0	↓
Rise Time	t_{4+}		5.0	8.5	5.0	8.5	7.0	9.5		5.0	8.5	5.0	8.5	6.0	9.0	
Fall Time	t_{4-}		5.0	8.0	5.0	8.0	7.0	9.0		5.0	8.0	5.0	8.0	6.0	8.5	
Propagation Delay	t_{1+3+}	3	4.0	7.5	4.0	7.5	6.0	↓		4.0	7.5	4.0	7.5	5.0	8.0	
	t_{1-3-}	↓	4.0	7.5	4.0	7.5	6.0			4.0	7.5	4.0	7.5	5.0	8.0	
Rise Time	t_{3+}		5.0	8.5	5.0	8.5	7.0	9.5		5.0	8.5	5.0	8.5	6.0	9.0	
Fall Time	t_{3-}		5.0	8.0	5.0	8.0	7.0	9.0		5.0	8.0	5.0	8.0	6.0	8.5	

* Individually test each input using the pin connections shown. † Individually test each output using the pin connections shown.

SWITCHING TIME TEST CIRCUIT @ 25°C

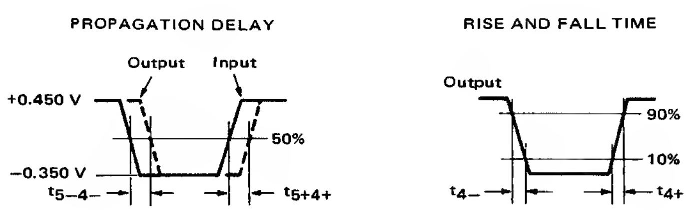


	@Test Temperature	V_{IL}	V_{IH}	$V_{IH\,max}$	V_{EE}	I_L
		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0%				mAdc
MC1229	−55°C	-1.580	-0.990	-	-5.2	-2.5
MC1229	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
MC1229	+125°C	-1.380	-0.700	-	-5.2	-2.5
MC1029	0°C	-1.525	-0.895	-	-5.2	-2.5
MC1029	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
MC1029	+75°C	-1.435	-0.775	-	-5.2	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Characteristic	Symbol	Pin Under Test	V_{IL}	V_{IH}	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	1, 5, 6, 7, 8, 13	-	14
Input Current	I_{in}	5	-	-	5	1, 6, 7, 8, 13	-	14
		8	-	-	8	1, 5, 6, 7, 13	-	↓
		1	-	-	1	5, 6, 7, 8, 13	-	↓
		6	-	-	6	1, 5, 7, 8, 13	-	↓
		13	-	-	13	1, 5, 6, 7, 8	-	↓
Input Leakage Current	I_R	5, 8*	-	-	-	1, 5, 6, 7, 8, 13	-	14
		1, 6, 13*	-	-	-	1, 5, 6, 7, 8, 13	-	14
Logical "1" Output Voltage	V_{OH} ‡	3, 11†	-	1	-	5, 6, 7, 8, 13	‡	14
		4, 9†	-	6	-	1, 5, 7, 8, 13	↓	↓
		2, 12†	-	13	-	1, 5, 6, 7, 8	↓	↓
		2, 3, 4†	-	5	-	1, 6, 7, 8, 13	↓	↓
		9, 11, 12†	-	8	-	1, 5, 6, 7, 13	↓	↓
Logical "0" Output Voltage	V_{OL}	3, 11†	1	-	-	5, 6, 7, 8, 13	-	14
		4, 9†	6	-	-	1, 5, 7, 8, 13	-	↓
		2, 12†	13	-	-	1, 5, 6, 7, 8	-	↓
		2, 3, 4†	5	-	-	1, 6, 7, 8, 13	-	↓
		9, 11, 12†	8	-	-	1, 5, 6, 7, 13		↓
Switching Times			**Pulse In**	**Pulse Out**		**V_{EE} = −4.0 Vdc**		**(+1.2 V)**
Propagation Delay	t_{5+4+}	4	5	4	-	1, 6, 7, 8, 13	-	14
	t_{5-4-}	↓	↓	↓		↓		↓
Rise Time	t_{4+}	↓	↓	↓		↓		↓
Fall Time	t_{4-}	↓	↓	↓		↓		↓
Propagation Delay	t_{1+3+}	3	1	3	-	5, 6, 7, 8, 13	-	↓
	t_{1-3-}	↓	↓	↓		↓		↓
Rise Time	t_{3+}	↓	↓	↓		↓		↓
Fall Time	t_{3-}	↓	↓	↓		↓		↓

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA). I_L applied to output under test.



Test circuit and waveforms show input pulse on pin 5 and output pulse on pin 4, however, all other input-output combinations tested in a similar manner will meet limits specified.

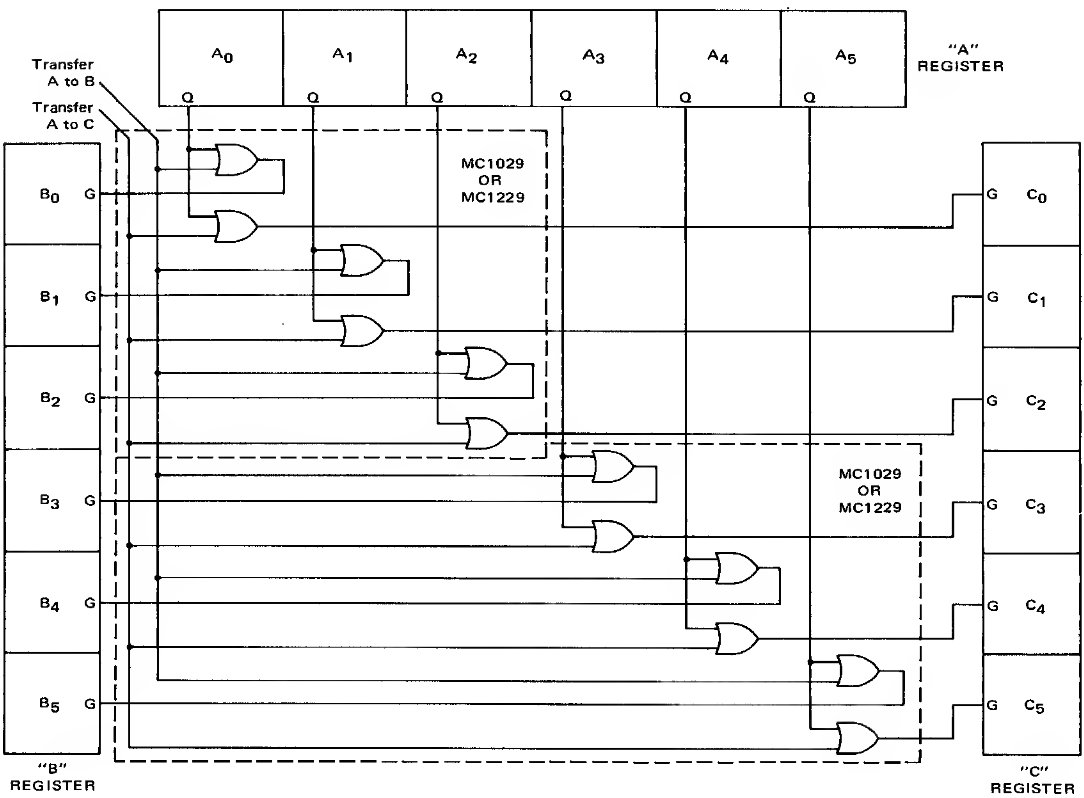
SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

The MC1029/MC1229 data distributor is a 2 X 3 array of 2-input OR gates, as shown in the logic diagram. Inputs X and Y may be used as control inputs to transfer the data on inputs A, B, and C, to the outputs on pins 9, 11, and 12, or to the outputs on pins 4, 3, and 2. Also, if it is desired to distribute data to three destinations, inputs X and Y may be used for data and A, B, and C as control inputs. The data distributor utilizes negative logic; i.e., the positive OR function becomes the negative AND. Data is transferred for a low level on the control inputs.

The data distributor is an example of the manner in which part of a logic system may be partitioned to reduce wiring and package count. Figure 1 illustrates the logic required for the transfer of data from "A" register to "B" register gating or to "C" register gating. Six stages per register are shown in the figure but arrays of any desired length may be built. The typical propagation delay of the data distributor in a system is 5.0 ns, permitting the rapid transfer of data through distribution gating. If data distribution is done on a double-rail basis instead of single-rail as shown, then twice the number of data distributors are required.

FIGURE 1 – REGISTER DATA TRANSFER



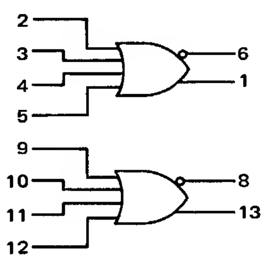
DUAL 4-INPUT
CLOCK DRIVER

MC1023

Provides simultaneous OR/NOR or AND/NAND output functions. It contains an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

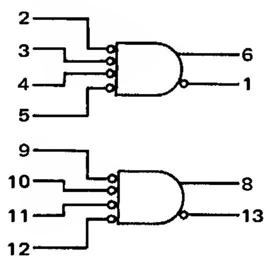
This circuit is designed to operate in high-speed digital computer applications as a clock driver or as a high-speed gate.

POSITIVE LOGIC



$6 = \overline{2 + 2 + 4 + 5}$
$1 = 2 + 3 + 4 + 5$

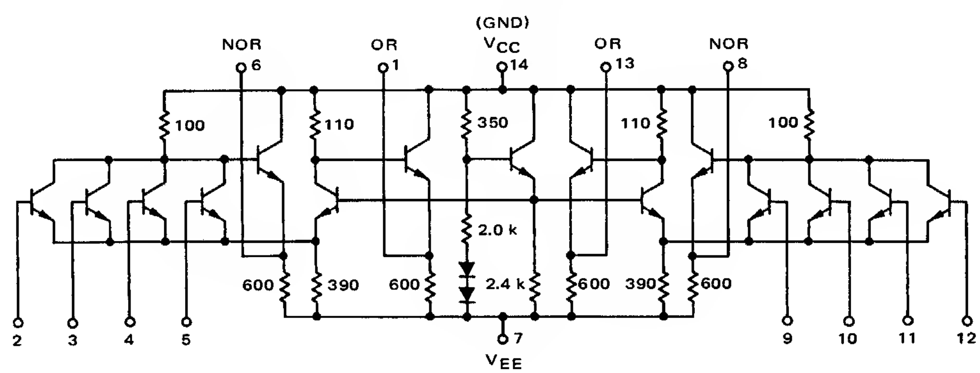
NEGATIVE LOGIC



$6 = \overline{2 \bullet 3 \bullet 4 \bullet 5}$
$1 = 2 \bullet 3 \bullet 4 \bullet 5$

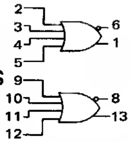
DC Input Loading Factor = 3
DC Output Loading Factor = 25
Power Dissipation = 250 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal.

ELECTRICAL CHARACTERISTICS



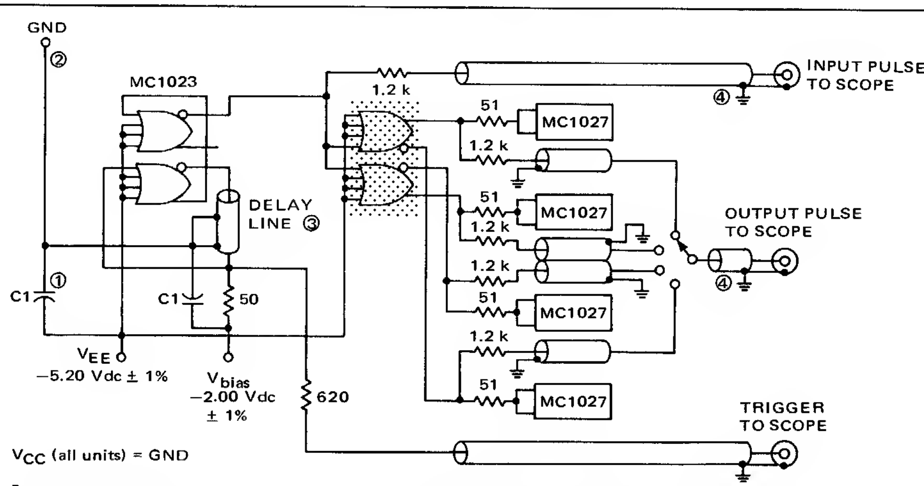
Test is shown for only one gate. The other gate is tested in the same manner.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{OL\,max}$	$V_{OH\,min}$	$V_{OH\,max}$	V_{EE}	mAdc I_L
0°C	-1.530	-0.930	-0.750	-5.2	-2.5
+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
+75°C	-1.440	-0.790	-0.635	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	MC1023P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{OL\,max}$	$V_{OH\,min}$	$V_{OH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	61	-	-	mAdc	-	-	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	14
Input Current	I_{in}	2	-	-	-	300	-	-	µAdc	-	-	2	3, 4, 5, 7, 9, 10, 11, 12	-	14
		3	-	-	-	↓	-	-	↓	-	-	3	2, 4, 5, 7, 9, 10, 11, 12	-	↓
		4	-	-	-	↓	-	-	↓	-	-	4	2, 3, 5, 7, 9, 10, 11, 12	-	↓
		5	-	-	-	↓	-	-	↓	-	-	5	2, 3, 4, 7, 9, 10, 11, 12	-	↓
Input Leakage Current	I_R	2	-	-	-	1.0	-	5.0	µAdc	-	-	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	14
		3	-	-	-	↓	-	↓	↓	-	-	-	↓	-	↓
		4	-	-	-	↓	-	↓	↓	-	-	-	↓	-	↓
		5	-	-	-	↓	-	↓	↓	-	-	-	↓	-	↓
"NOR" Logical "1" Output Voltage ‡	V_{OH} ‡	6	-0.930	-0.750	-0.850	-0.700	-0.790	-0.635	Vdc	2	-	-	3, 4, 5, 7, 9, 10, 11, 12	6	14
			↓	↓	↓	↓	↓	↓	↓	3	-	-	2, 4, 5, 7, 9, 10, 11, 12	↓	↓
			↓	↓	↓	↓	↓	↓	↓	4	-	-	2, 3, 5, 7, 9, 10, 11, 12	↓	↓
			↓	↓	↓	↓	↓	↓	↓	5	-	-	2, 3, 4, 7, 9, 10, 11, 12	↓	↓
"NOR" Logical "0" Output Voltage	V_{OL}	6	-2.050	-1.530	-2.000	-1.500	-1.940	-1.440	Vdc	-	2	-	3, 4, 5, 7, 9, 10, 11, 12	-	14
			↓	↓	↓	↓	↓	↓	↓	-	3	-	2, 4, 5, 7, 9, 10, 11, 12	-	↓
			↓	↓	↓	↓	↓	↓	↓	-	4	-	2, 3, 5, 7, 9, 10, 11, 12	-	↓
			↓	↓	↓	↓	↓	↓	↓	-	5	-	2, 3, 4, 7, 9, 10, 11, 12	-	↓
"OR" Logical "1" Output Voltage ‡	V_{OH} ‡	1	-0.930	-0.750	-0.850	-0.700	-0.790	-0.635	Vdc	-	2	-	3, 4, 5, 7, 9, 10, 11, 12	6	14
			↓	↓	↓	↓	↓	↓	↓	-	3	-	2, 4, 5, 7, 9, 10, 11, 12	↓	↓
			↓	↓	↓	↓	↓	↓	↓	-	4	-	2, 3, 5, 7, 9, 10, 11, 12	↓	↓
			↓	↓	↓	↓	↓	↓	↓	-	5	-	2, 3, 4, 7, 9, 10, 11, 12	↓	↓
"OR" Logical "0" Output Voltage	V_{OL}	1	-2.050	-1.530	-2.000	-1.500	-1.940	-1.440	Vdc	2	-	-	3, 4, 5, 7, 9, 10, 11, 12	-	14
			↓	↓	↓	↓	↓	↓	↓	3	-	-	2, 4, 5, 7, 9, 10, 11, 12	-	↓
			↓	↓	↓	↓	↓	↓	↓	4	-	-	2, 3, 5, 7, 9, 10, 11, 12	-	↓
			↓	↓	↓	↓	↓	↓	↓	5	-	-	2, 3, 4, 7, 9, 10, 11, 12	-	↓
Switching Times			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out				
Propagation Delay (Fan-Out = 2)*	t_{5+6-}	6	2.0	3.5	2.0	3.5	3.0	4.5	ns	5	6	-	2, 3, 4, 7, 9, 10, 11, 12	-	14
	t_{5-6+}	6	2.0	3.0	2.0	3.0	3.0	4.0	↓	↓	6	-	↓	-	↓
	t_{5+1+}	1	2.0	3.0	2.0	3.0	3.0	4.0	↓	↓	1	-	↓	-	↓
	t_{5-1-}	1	2.0	3.5	2.0	3.5	3.0	4.5	↓	↓	1	-	↓	-	↓
(Fan-Out = 10)*	t_{5+6-}	6	2.5	3.5	2.5	3.5	3.0	5.0	↓	↓	6	-	↓	-	↓
	t_{5-6+}	6	2.0	3.5	2.0	3.5	3.0	5.0	↓	↓	6	-	↓	-	↓
	t_{5+1+}	1	2.0	3.5	2.0	3.5	3.0	5.0	↓	↓	1	-	↓	-	↓
	t_{5-1-}	1	2.5	3.5	2.5	3.5	3.0	5.0	↓	↓	1	-	↓	-	↓
Rise Time (Fan-Out = 2)*	t_{6+}	6	2.0	4.0	2.0	4.0	3.5	5.0	↓	↓	6	-	↓	-	↓
	t_{1+}	1	2.0	4.0	2.0	4.0	3.5	5.0	↓	↓	1	-	↓	-	↓
(Fan-Out = 10)*	t_{6+}	6	3.0	5.5	3.0	5.5	5.0	7.5	↓	↓	6	-	↓	-	↓
	t_{1+}	1	3.0	5.5	3.0	5.5	5.0	7.5	↓	↓	1	-	↓	-	↓
Fall Time (Fan-Out = 2)*	t_{6-}	6	2.0	4.5	2.0	4.5	3.0	5.5	↓	↓	6	-	↓	-	↓
	t_{1-}	1	2.0	4.5	2.0	4.5	3.0	5.5	↓	↓	1	-	↓	-	↓
(Fan-Out = 10)*	t_{6-}	6	3.0	5.5	3.0	5.5	5.0	7.5	↓	↓	6	-	↓	-	↓
	t_{1-}	1	3.0	5.5	3.0	5.5	5.0	7.5	↓	↓	1	-	↓	-	↓

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA). * A fan-out is defined as one $\bar{J}$ or $\bar{K}$ input.

SWITCHING TIME TEST CIRCUIT

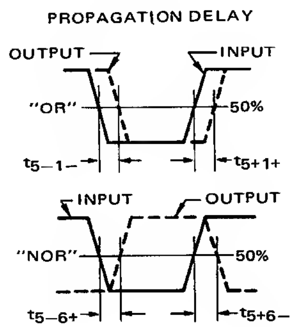


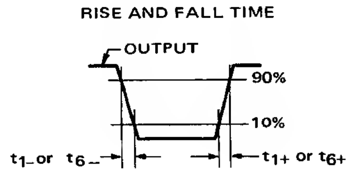
① C1 = 1.0 µF ± 10% in parallel with 0.001 µF ± 10%

② All leads to ground as short as possible

③ Delay line = 10 ft P D Electronics CT. 070-50 miniature coaxial cable or equivalent. Other internal fixture cables are same type.

④ All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Plug directly into 50-ohm input of scope.





Waveforms shown for pulse in on pin 5, pulse out on pin 1 or pin 6. Other input-output combinations will meet the limits specified.

APPLICATIONS INFORMATION

The MC1023 is a dual high-speed gate designed for use as a clock driver which allows the MECL II flip-flops to operate at their full speed capability. More advanced processing techniques than those used on standard MECL II are employed for the clock driver, resulting in an improved speed-power product. The dual gate exhibits typical propagation delay times of 2.0 ns. Due to this short propagation delay, the gate makes an ideal clock driver for long shift registers where the clock pulse may be distributed with minimal skew time over the entire register length.

Since rise and fall times may be as fast as 1.0 ns under light loading, the following precautions must be taken during layout. The MC1023 will not drive back-plane point-to-point wiring satisfactorily. Due to the fast logic transitions a maximum length of three inches for point-to-point wiring is recommended. Lower impedance printed wires allow longer line lengths. Due to the low output impedance (5.0 ohms) of the MC1023, additional terminating resistance to −5.2 V may be employed. This reduces fall time for capacitive loads and propagation delay to negative-going outputs. Figure 1 shows typical curves for output voltage versus load current. Figures 2 through 7 show curves for rise, fall, and propagation delay times versus loading for a typical gate. Capacitance of 5.0 pF per fan-out was used during the tests. This is conservative, since stray and input capacitance is closer to 4.0 pF per fan-out when driving flip-flops in high-speed designs.

The MC1023 is also very useful for providing the additional levels of gating required for some counting configurations such as divide-by-seven and divide-by-thirteen counters. The maximum frequency of operation of such a counter depends upon the flip-flop and gating delay which determines the minimum "up time" of the clock waveforms. Due to its short propagation delay the MC1023 when used with an MC1027 allows a divide-by-seven counter to operate up to 100 MHz.

Due to the 5.0-ohm output impedance the clock driver will also drive low impedance lines. When driving a 50-ohm termination to −2.0 V the output "1" level will be reduced by a maximum of 0.100 V. The minimum "1" level is approximately −0.950 V with a load current of 21 mA, reducing voltage noise immunity by 0.100 V. Noise power or energy noise immunity is still good due to the very low gate output impedance and low line impedance.

Two additional applications of the MC1023 are shown in Figures 8 and 9.

FIGURE 1 - TYPICAL OUTPUT CHARACTERISTICS

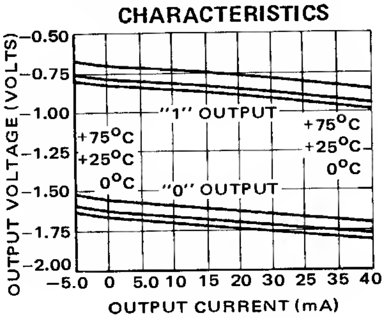


FIGURE 2 - RISE TIME

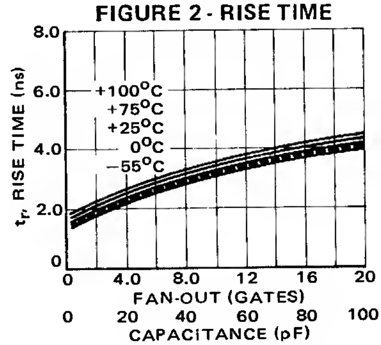
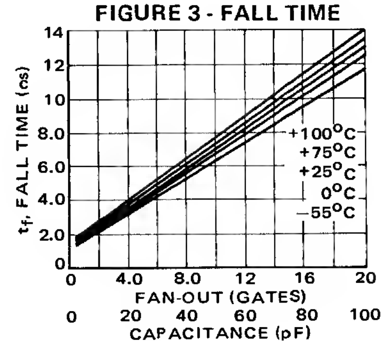


FIGURE 3 - FALL TIME



APPLICATIONS INFORMATION (continued)

FIGURE 4 - t_{pd+-}

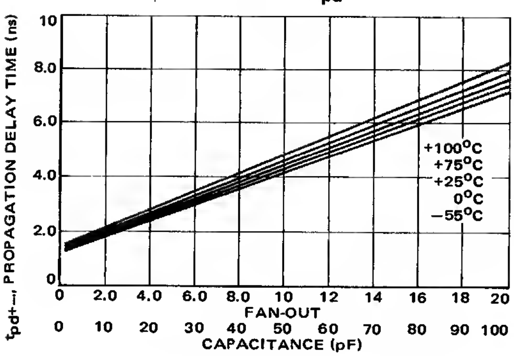


FIGURE 5 - t_{pd-+}

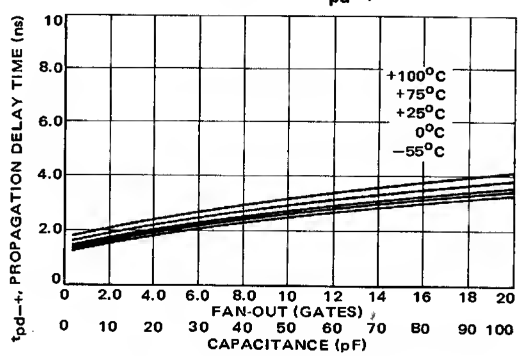


FIGURE 6 - t_{pd++}

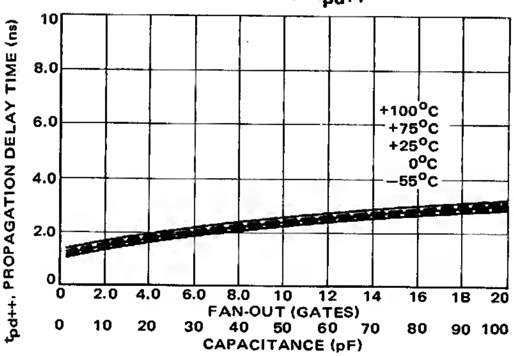


FIGURE 7 - t_{pd--}

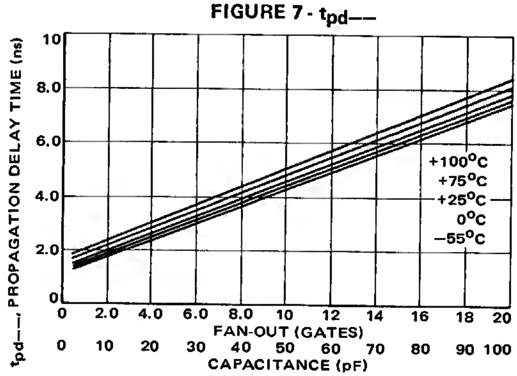
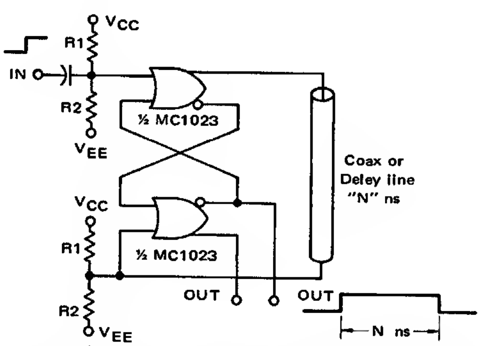


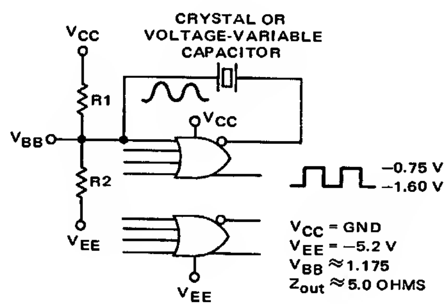
FIGURE 8 - MC1023 AS A ONE SHOT AND CLOCK SHAPER



Uniform pulse determined only by delay "N". The circuit is very useful for generating accurate and stable pulse widths or reshaping clock pulse width. Pulse widths down to 3.0 ns are obtainable.

Circuit courtesy of Mr. O. Gene Gabbard, Member of Technical staff, Communications Satellite Corporation.

FIGURE 9 - MC1023 AS A CRYSTAL OSCILLATOR



Power Dissipation = ¼ Watt
The Gate is Useful to 150+ MHz

For specific frequencies of operation, the crystal feedback may be obtained from the OR output. For further information see Application Note AN-417.